MODULATION, CONTROL, AND APPLICATIONS OF MULTILEVEL CONVERTERS FOR POWER SYSTEMS WITH HIGH PENETRATION OF WIND ENERGY

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MODULATION, CONTROL, AND APPLICATIONS OF MULTILEVEL CONVERTERS FOR POWER SYSTEMS WITH HIGH PENETRATION OF WIND ENERGY

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To my dear parents and sister

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LIST OF ABBREVIATIONS

ADF-PWM	Adaptive doubled frequency PWM
ANPC	Active neutral-point-clamped
CCS	Code Composer Studio
DAC	Digital-to-analog converter
DCC	Diode-clamped converter
DFIG	Doubly-fed induction generator
DF-PWM	Doubled frequency PWM
DSP	Digital signal processor
DTC	Direct torque control
FACTS	Flexible AC transmission systems
FOC	Field oriented control
GSC	Grid side converter
HVDC	High voltage direct current
IGBT	Insulated-gate bipolar transistor
MMC	Modular multilevel converter
MPC	Model predictive control
MPPT	Maximum-power-point-tracking
NLM	Nearest-level modulation
NPC	Neutral-point-clamped
PI	Proportional-integral
PWM	Pulse width modulation
RSC	Rotor side converter
SG	Synchronous generator
SM	Submodule

SOA	Safe operating area
STATCOM	Static synchronous compensator
SVM	Space vector modulation
VC	Vector control
WECS	Wind-energy conversion systems

SUMMARY

Power electronic converters are widely adopted in modern wind energy generation and transmission systems. Resulting from the increasing sizes of wind turbines and wind farms, multilevel converters are required to overcome the voltage and current limits of the power semiconductors. The proposed research focuses on developing modulation and control methods for multilevel converters so as to optimize their applications in wind energy generation and transmission.

Among various pulse width modulation (PWM) methods for multilevel converters, space vector modulation (SVM) provides more flexibility to optimize switching waveforms, but requires more complicated implementation because it simultaneously deals with all phases. This dissertation first establishes the inherent relationship between the SVM and a phase-voltage modulation technique (called the nearest-level modulation): the two modulation methods are functionally equivalent. Consequently, a simplified SVM scheme for multilevel converters is proposed, which is independent of the level number of the converter and for the first time achieves the same easy implementation as phase-voltage modulation techniques. Based on two orthogonal unit-vectors that decouple the components of different phases, the proposed scheme can potentially be extended to multiphase multilevel applications.

The three-level active neutral-point-clamped (ANPC) converter is well suited to control high-power wind turbine generators, but suffers from unequal power loss distribution among its semiconductor devices. This dissertation proposes a new modulation scheme, called the adaptive doubled frequency PWM (ADF-PWM), to achieve the power loss balancing control for the ANPC converter. The basic idea of the proposed scheme is adaptively adjusting the duty cycles of the switching states for every switching cycle, so as to optimize the power loss distribution. This dissertation also

demonstrates that low fundamental frequencies further aggravate the converters' power loss and junction temperature unbalance. Since the proposed ADF-PWM scheme optimizes the power loss distribution for every switching cycle, both average and instantaneous/peak junction temperatures of the most stressed semiconductors are reduced by the ADF-PWM scheme, especially at low fundamental frequencies.

In applications of high voltage direct current (HVDC) transmission systems connecting large wind farms over a long distance to a utility network, the modular multilevel converter (MMC) is the best choice, because of its modularity and scalability to meet any voltage level requirements. It is imperative to regulate the MMC's submodule (SM) capacitor voltages, for the sake of proper operation of the MMC. At the same time, circulating currents have to be well controlled because of their significant influence on the ratings and power losses of the MMC. This dissertation proposes an optimized control method for the MMC based on the proposed simplified SVM scheme, which significantly improves the capacitor voltage balancing and circulating current suppression. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed method is well suited to the MMC with a large number of SMs.

CHAPTER 1 INTRODUCTION AND RESEARCH OBJECTIVES

1.1 Background of Wind Energy Generation

Wind energy generation has grown rapidly around the world, resulting mostly from increasing concerns about energy security and sustainability. In the U.S., a scenario of wind energy contributing 20% of the total energy supply by 2030 is envisioned by the Department of Energy [1]. In some countries, the penetration of wind energy has reached high levels of the electricity supply. For example, in Denmark (34%) and Spain (21%), wind energy has become the largest source of electricity [2]. World wind energy capacity reached 319 GW by the end of 2013, contributing close to 4% to the global electricity demand; today 103 countries are using wind energy on commercial basis [3]. By the end of 2018, about 600 GW of worldwide wind installations are expected [4].

1.1.1 Wind Energy Conversion Systems

Variable-speed wind energy conversion systems (WECSs), based on power electronic converters, are commonly adopted in modern wind energy plants to maximize capturing energy from the wind. Two major configurations of variable-speed WECSs have been developed [5] [6]: 1) WECSs equipped with doubly-fed induction generators (DFIGs) and partially-rated converters, as shown in Figure 1.1 (also referred to as Type 3 systems) ; and 2) WECSs equipped with synchronous generators (SGs) and fully-rated converters, as shown in Figure 1.2 (also referred to as Type 4 systems).

Because of the partially rated converter (approximately 30% of the total power) and thus a reduced cost, the DFIG configuration has been the most widely adopted by industry. The SG configuration is also attracting increased attention recently, benefiting from a simple control strategy and a wide variable-speed range for optimal operation. However, whichever configuration is adopted, the continuous increase in size and power

rating of wind turbines (and wind turbine generators) introduces more challenges to the power electronic converters. The largest wind turbine generators today are rated at 8 MW (Type 4 systems with permanent magnet SGs) [7].

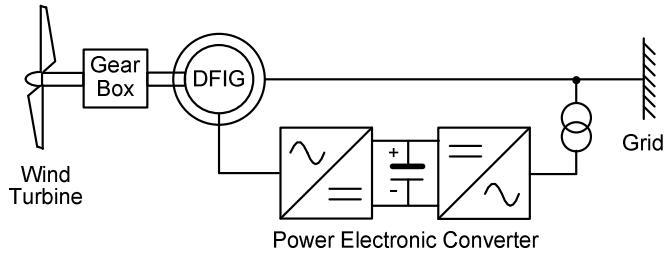


Figure 1.1 A WECS using a DFIG and a partially-rated converter.

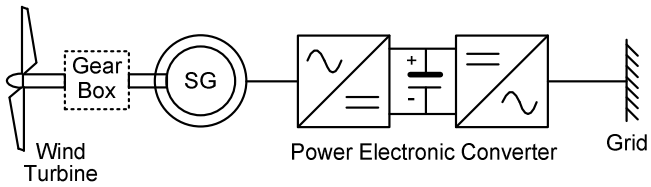


Figure 1.2 A WECS using a SG and a fully-rated converter.

1.1.2 Wind Power Transmission

A wind farm normally consists of numerous wind turbines to gain the desired power production capacity. For example, the currently largest wind farm in the U.S. is the Alta Wind Energy Centre (AWEC) in Tehachapi, California, USA, which has 600 wind turbines and reaches an operational capacity of 1,548 MW [8]. Figure 1.3 illustrates the typical configuration of a wind farm [9]. The total power of all the wind turbines is fed to a collector bus through several collector feeders (underground cables). Each wind turbine generator's terminal voltage typically ranges from 575 to 690 V (line-to-line), and a local generator transformer typically steps this up to 12.1 to 34.5 kV (line-to-line) according to the collector bus. To connect the wind farm to the transmission system, a main transformer typically increases this to 169 or 345 kV (line-to-line) depending on the total size of the wind farm and the distance to the point of common coupling (PCC) with the nearest utility grid.

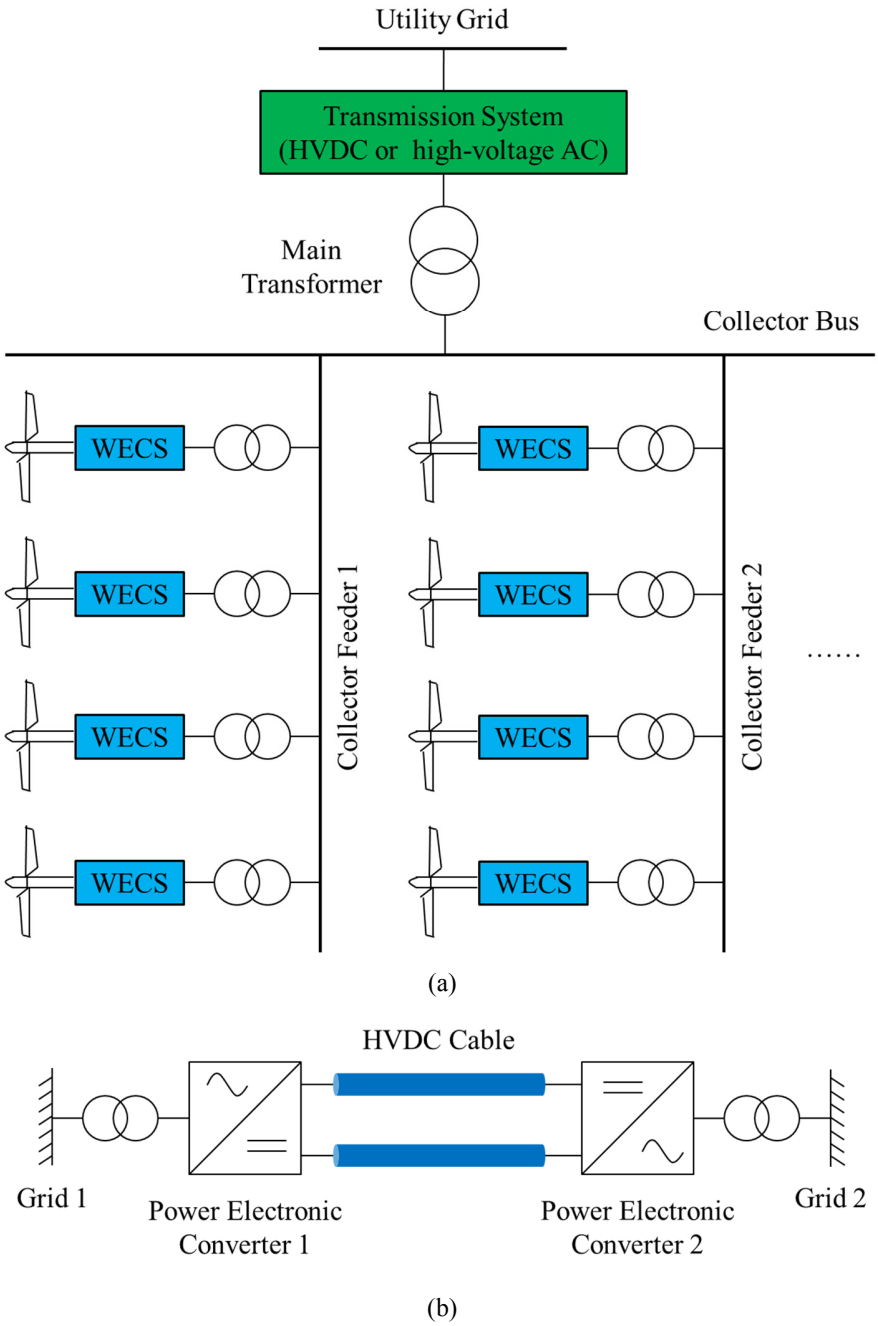


Figure 1.3 The typical configuration of a wind farm: (a) overall system; (b) HVDC system.

Compared with the traditional energy transportation systems using overhead transmission lines, the high voltage direct current (HVDC) technique [10] typically as in Figure 1.3(b) offers a more efficient and cost-effective way to deliver the wind energy particularly over longer distances between the wind farm and the utility.

Furthermore, flexible AC transmission systems (FACTS), such as static synchronous compensators (STATCOMs), are usually adopted at some critical buses to ensure the grid voltage stability, since high penetration of wind energy introduces high uncertainty and variability to the power system. Both HVDC and FACTS systems require high-voltage high-power converters.

1.1.3 Summary of Challenges and Candidate Solutions

The increasing sizes of wind turbines and wind farms challenge the power electronic converters, since a high-power rating implies a high voltage or current stress on the converter. Considering the voltage/current limits of existing power semiconductors, the traditional two-level converters are reaching the upper limits of either the current or voltage ratings of the power semiconductor switching devices.

One way to extend the voltage and power ranges of the two-level topology is to use parallel-connected power semiconductors (for high-current applications) or series-connected power semiconductors (for high-voltage applications) [11]-[13]. However, an inherent problem of this approach is that additional auxiliary circuits are normally required in order to balance the voltage/current sharing among the series/parallel-connected power semiconductors. These additional auxiliary circuits not only increase the cost of the converter, but also complicate the converter's control.

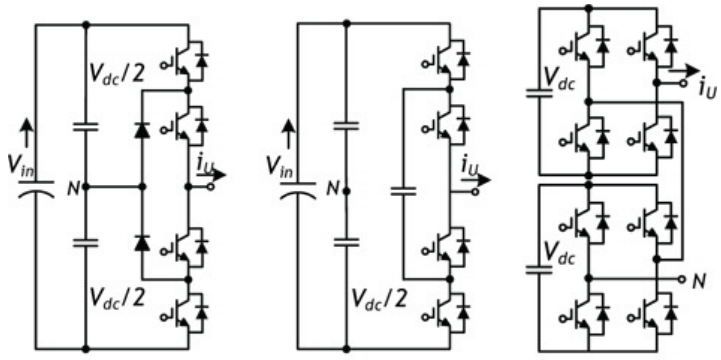
Multilevel converters (introduced later in detail) represent another solution to overcome the voltage and current limits of the power semiconductors [14]. Compared with using series/parallel-connected power semiconductors, multilevel converters avoid the damages caused by the diversity among the characteristics of the power semiconductors. Moreover, the high-voltage operation achieved by multilevel converters leads to lower currents, and therefore a reduced size and cost of cables and line filters. Generating lower voltage/current harmonics is another significant advantage of multilevel converters.

1.2 Background of Multilevel Converters

1.2.1 Topologies

During the past decades, three basic topologies have been proposed for multilevel converters: diode-clamped (neutral-clamped) [15]-[17], capacitor-clamped (flying capacitors) [18], and cascaded H-bridge with separate dc sources [19]. Figure 1.4 illustrates the single-phase circuit diagram of each basic topology.

Figure 1.5 shows another emerging topology called the modular multilevel converter (MMC), which was introduced in the early 2000s [20] and has recently been shown to be even more promising for high-voltage/power applications, due to its significant merits such as modularity and scalability to meet any voltage level requirements [21]-[23]. For example, the first commercialized MMC-based HVDC system, i.e., the "Trans Bay Cable Project", is reported to have achieved ±200 kV/400 MW and 216 voltage-levels [24].



(a) (b) (c)

Figure 1.4 Three basic multilevel converter topologies: (a) diode-clamped; (b) flying capacitors; and (c) cascaded H-bridge.

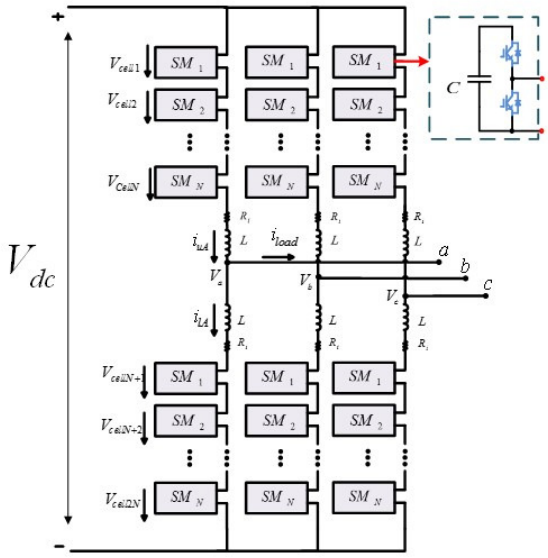


Figure 1.5 Circuit diagram of the MMC.

Among the three basic multilevel topologies, the diode-clamped converter (DCC) or also called neutral-point-clamped (NPC) converter has attracted much attention because of its simple circuit structure. The three-level NPC converter or its derivative (introduced later) is particularly suited to control a single wind turbine generator, considering the voltage (<6.6 kV) and power (<10 MW) ranges of existing wind turbine generators.

On the other hand, the HVDC transmission system connecting a large wind farm to a distant utility network can reach up to 800 kV and 8 GW [25], so the MMC topology is the best choice in this application. Nowadays most commercialized HVDC systems are based on the MMC [26].

1.2.2 Modulation Methods

Many pulse width modulation (PWM) methods have been developed for multilevel converters, and most of them can be classified into three typical categories: 1) carrier-based modulation, including phase-shifted PWM [27]-[30] and phase-disposition PWM [31]-[33]; 2) nearest-level modulation (NLM) [34]-[38]; and 3) space vector modulation (SVM) [39]-[44].

SVM works with line-to-line voltages (i.e., it simultaneously deals with all phases), while the other two methods are phase-voltage modulation techniques. Since SVM eliminates the influence of common-mode voltages and avoids the use of any triangular carrier wave, it conveniently provides more flexibility (i.e., redundant switching sequences and adjustable duty cycles) to optimize switching waveforms [38] [44], and is more suited to digital implementations. These advantages of SVM can lead to a significantly improved performance of multilevel converters, especially when the level number of the converter is large (e.g., 216 voltage-levels as in the "Trans Bay Cable Project"), because a larger level number facilitates a higher redundancy and therefore more potential for optimization.

However, in spite of its distinct advantages, SVM for four or higher level converters is difficult. There generally are n^3 switching states and $6(n\text{-}1)^2$ triangles in the space vector diagram of a three-phase n-level converter [44]; a reference vector can be located within any triangle. For example, Figure 1.6 shows the space vector diagram of a five-level converter [44]. To achieve the same volt-second average as the reference vector $\boldsymbol{V}_{\text{ref}}$, it is the task of SVM to select suitable switching states of the located triangle $\Delta P_1P_2P_3$ (its vertices are the "nearest three vectors" $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$) and execute them for respective needed durations (duty cycles) in an appropriate sequence (switching sequence). In order to carry out the real-time control for a converter with a large number of levels (e.g., in MMC and HVDC applications), an SVM scheme is required to be easily implementable and computationally efficient. Nevertheless, none of the earlier SVM methods [39]-[44] are well suited to meet those requirements. A further simplified SVM scheme is therefore needed.

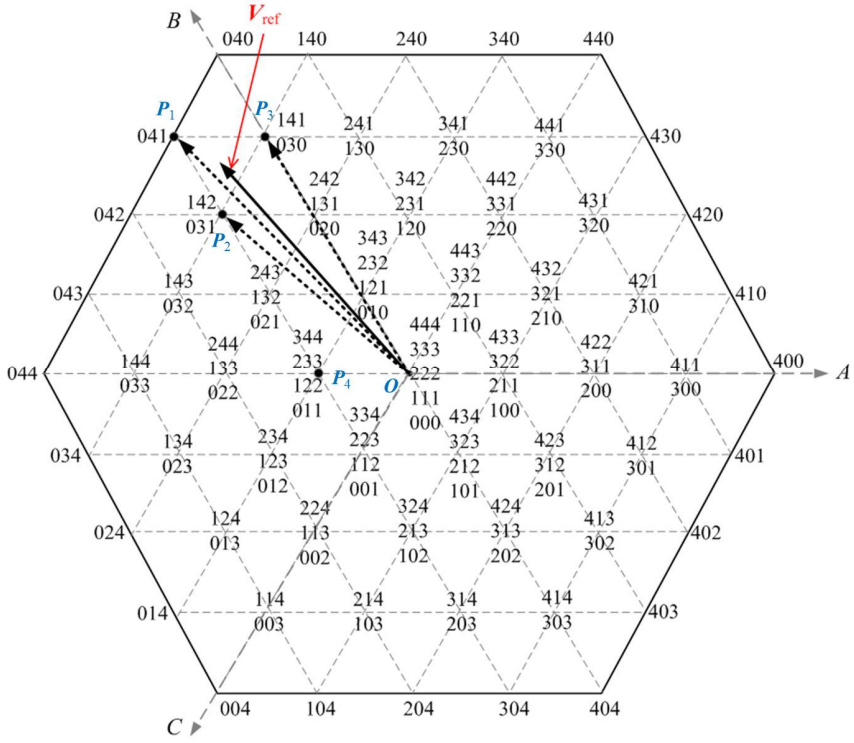


Figure 1.6 Space vector diagram of a five-level converter.

1.2.3 Control and Operational Issues

The capacitor voltage unbalance [17] is one of the most well-known problems existing in NPC topologies of four and more levels. On the other hand, for three-level NPC converters this voltage unbalance problem has been solved and several solutions have been reported [45]. Three-level NPC converters are widely adopted by the industry and are commercialized by at least nine manufacturers [10].

Nevertheless, a remaining major drawback of the three-level NPC converter is the unequal power loss distribution among the semiconductors [46]. The unbalanced power losses cause unequal junction temperatures of the semiconductors; as a result some power devices become much hotter than others, or experience significantly larger junction temperature ripples. Both the power rating and lifetime of the converter are therefore limited by the most stressed devices. To overcome the loss unbalance problem of the NPC converter, the active NPC (ANPC) technique was introduced in 2001 [47], but it has

been demonstrated [48] that in many cases, the conventional modulation method for the ANPC converter only marginally relieves the loss unbalance problem.

For the MMC, it is also imperative to regulate the submodule (SM) capacitor voltages, for the sake of proper operation of the MMC. Furthermore, reducing the capacitor voltage ripples is always an important objective because it enables the use of smaller capacitors [49]. This eventually leads to a reduced cost of the MMC considering the large number of SM capacitors. At the same time, circulating currents have to be well controlled because of their significant influence on the ratings and power losses of the MMC. Since the SM capacitor voltages are mutually coupled with the circulating currents within the same phase leg of the MMC, the control of the MMC becomes complicated. The control of both capacitor voltages and circulating currents, which is considered as the internal control of the MMC since it should not affect the MMC's response to outside circuits, is typically achieved at the modulation stage.

1.3 Objectives of Research

The proposed research focuses on the following aspects, in order to provide solutions for the continuously increasing power ratings of wind turbines and wind farms:

- Modulation methods for multilevel converters, especially the SVM scheme, since SVM provides more flexibility than other modulation methods to optimize the converters' performance.
- Power loss balancing method for three-level ANPC converters, in order to control high-power wind turbine generators and enhance the lifetimes and safe operating areas (SOAs) of the converters.
- Control of capacitor voltages and circulating currents for the MMC, which is crucial to wind power HVDC transmission for large wind farms.

1.4 Dissertation Outline

The rest of this dissertation is organized as follows:

Chapter 2 provides a comprehensive literature review on the existing methods and techniques related to the proposed research.

Chapter 3 investigates the inherent relationship between the SVM and NLM (nearest-level modulation) modulation methods, which facilitates the simplification of the SVM scheme for multilevel converters.

Chapter 4 proposes a simplified SVM scheme for multilevel converters. The proposed SVM scheme achieves the same easy implementation as the NLM, while maintaining significant flexibility (i.e., redundant switching sequences and adjustable duty cycles). Therefore, it is well suited to large level-number applications (e.g., MMC and HVDC).

Chapter 5 presents an improved modulation scheme for power loss balancing control of three-level ANPC converters.

Chapter 6 proposes an optimized control of the MMC based on the simplified SVM scheme, which represents a general framework for implementing SVM-based control for the MMC.

Chapter 7 summarizes the conclusions and contributions of this dissertation work and recommendations for future investigations.

CHAPTER 2 REVIEW OF LITERATURE

This chapter provides a literature review on the existing techniques related to this dissertation work, including: 1) modelling and control methods for wind turbines and doubly-fed induction generators (DFIGs); 2) space vector modulation (SVM) methods for multilevel converters; 3) power loss balancing schemes for three-level active neutral-point-clamped (ANPC) converters; 4) modulation and control methods for the modular multilevel converter (MMC).

2.1 Modelling and Control of DFIG-Based Wind Energy Generation

2.1.1 Modeling and Operation of Wind Turbines

The mechanical power captured by a wind turbine is expressed as [50] [51]

$$P_m = P_{wind} C_P(\lambda, \theta) = \frac{1}{2} \rho A_r v_w^3 C_P(\lambda, \theta) \tag{2.1}$$

where P_{wind} is the wind power in W, C_P is the power coefficient, ρ is the air density in kg/m^3, A_r is the area swept by the turbine rotor blades in m^2, and v_w is the wind speed in m/s. The power coefficient depends on the blade pitch angle θ, and the tip-speed ratio λ defined by

$$\lambda = \frac{\omega_t R}{v_w} \tag{2.2}$$

where R is the blade length in m and ω_t is the turbine rotating speed in rad/s. As a complex nonlinear function that depends on the blade design, the C_P-λ-θ relationship is usually given by wind-turbine manufacturers. Figure 2.1 shows the C_p curves of a 3.6 MW wind turbine, where a polynomial is used to approximate the actual C_P-λ-θ relationship [50].

Figure 2.2 shows a typical output-power curve of wind turbines. For the purposes of efficiency and safety, wind turbines operate only when the wind speed is between the cut-in and cut-out speeds. Particularly, when the wind speed is between the cut-in and rated speeds, wind turbines are typically operated in a maximum-power-point-tracking (MPPT) mode, and the turbines are controlled such that C_p reaches its peak value. If the wind speed increases above the rated value, then a control loop, called the pitch angle control, is activated to increase the pitch angle θ, so as to maintain the captured wind power within the turbine rating.

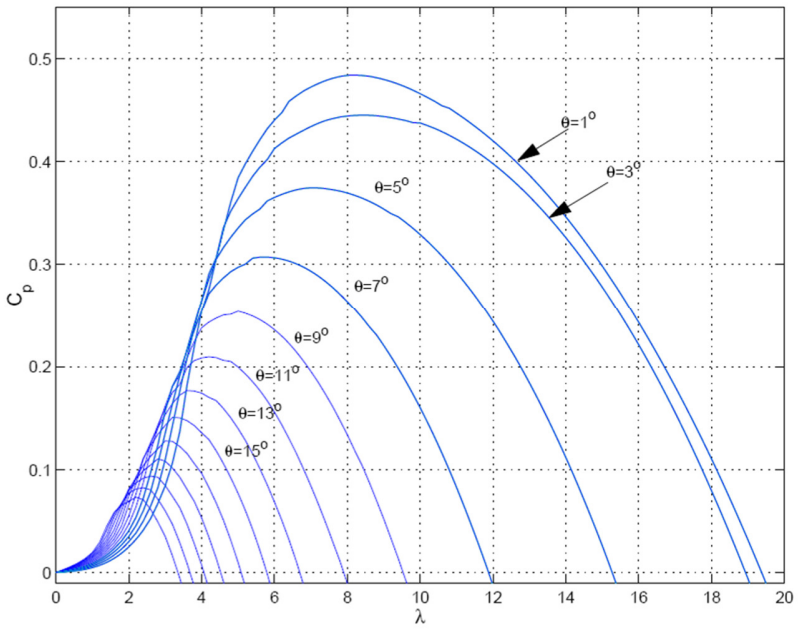


Figure 2.1 Typical wind-turbine C_p curves [50].

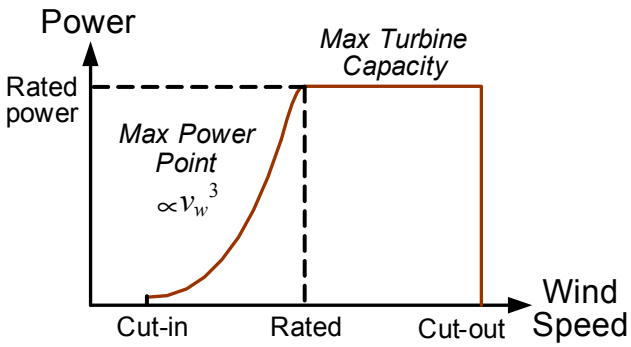


Figure 2.2 Typical wind-turbine power curve.

2.1.2 Field Oriented Control for DFIGs

The control of wind energy conversion systems (WECSs) is demonstrated in this section based on the DFIG configuration shown in Figure 1.1, since it has been the most widely adopted by industry. Two major control methods have been introduced to control DFIGs: the field oriented control (FOC) or vector control (VC) [52]-[54], and the direct torque control (DTC) [55]. DTC has good dynamic performance, and requires no knowledge of system parameters. However, compared to DTC, it is much easier for FOC to extend from the two-level to a multilevel application [10]. The reason is that DTC controls the electromagnetic torque (or active power) and the flux magnitude (or reactive power) by selecting a voltage space vector or switching state. As mentioned in Chapter 1, the number of switching states increases significantly with the increase in voltage levels. This section therefore focuses on the FOC-based control scheme for the DFIG.

As shown in Figure 1.1, the power electronic converters of a DFIG-based WECS consist of a rotor-side converter (RSC) and a grid-side converter (GSC). The RSC controls the DFIG-stator active (or rotor speed or electromagnetic torque of the DFIG) and reactive power outputs, while the GSC maintains the dc-link voltage and may be controlled to provide additional reactive power to the grid.

In the stator-flux oriented reference frame, the *d*-axis is aligned with the stator flux linkage vector (i.e., the *q*-axis stator flux linkage $\lambda_{qs} = 0$), and the following relationships are found for the RSC [56]:

$$T_e = -\frac{3}{2}\frac{P}{2} L_m^2 i_{ms} i_{qr} / L_s \tag{2.3}$$

$$Q_s = \frac{3}{2}\omega_s L_m^2 i_{ms}(i_{ms} - i_{dr}) / L_s \tag{2.4}$$

$$v_{dr} = r_r i_{dr} + \sigma L_r \frac{di_{dr}}{dt} - s\omega_s \sigma L_r i_{qr} \tag{2.5}$$

$$v_{qr} = r_r i_{qr} + \sigma L_r \frac{di_{qr}}{dt} + s\omega_s \left(\sigma L_r i_{dr} + L_m^2 i_{ms} / L_s\right) \tag{2.6}$$

where all symbols have their usual meanings and

$$i_{ms} = \frac{\lambda_{ds}}{L_m} \tag{2.7}$$

$$\sigma = 1 - \frac{L_m^2}{L_s L_r} \tag{2.8}$$

The stator magnetizing current i_{ms} is considered constant, since the stator is connected to the grid and the influence of the stator resistance is small (i.e., the stator flux linkage is constant). It is observed from (2.3) and (2.4) that the electromagnetic torque T_e (or the DFIG rotor speed ω_r) can be controlled by regulating the q-axis rotor current i_{qr}, while the stator reactive power Q_s can be controlled by regulating the d-axis rotor current i_{dr}. Consequently, Figure 2.3 shows the FOC control scheme of the RSC [54] [56], where the compensation terms v_{dr2} and v_{qr2} are added to accelerate the tracking of the d- and q-axis rotor currents according to (2.5) and (2.6).

The FOC control scheme of the GSC [54] [56] can be similarly obtained and is shown in Figure 2.4. The dc-link voltage v_{dc} is controlled by regulating the d-axis grid current i_{dg} (from the grid to the GSC), while the grid voltage V_s (or the reactive power delivered from the GSC to the grid) is controlled by regulating the q-axis grid current i_{qg}.

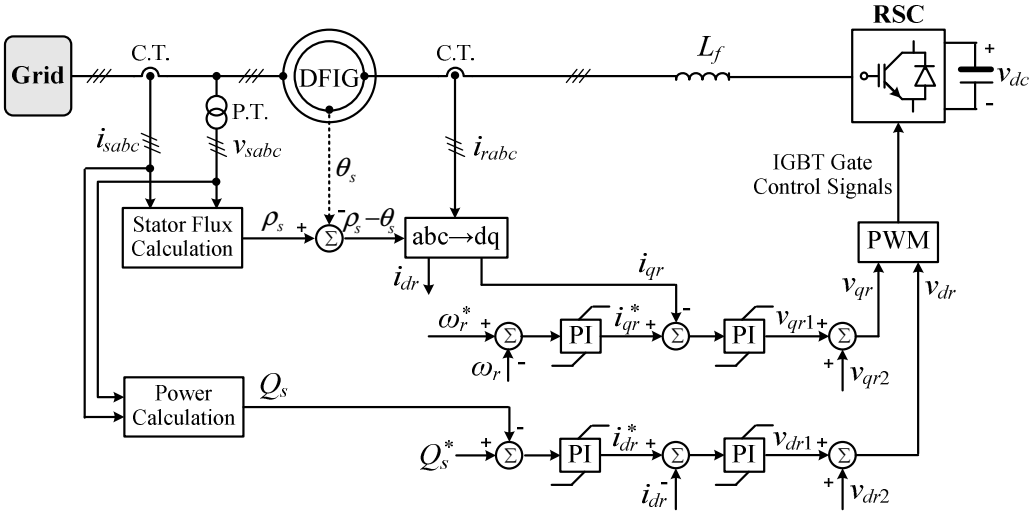


Figure 2.3 Overall FOC control scheme of the RSC: $v_{dr2} = -s\omega_s\sigma L_r i_{qr}$, $v_{qr2} = s\omega_s(\sigma L_r i_{dr} + L_m^2 i_{ms}/L_s)$.

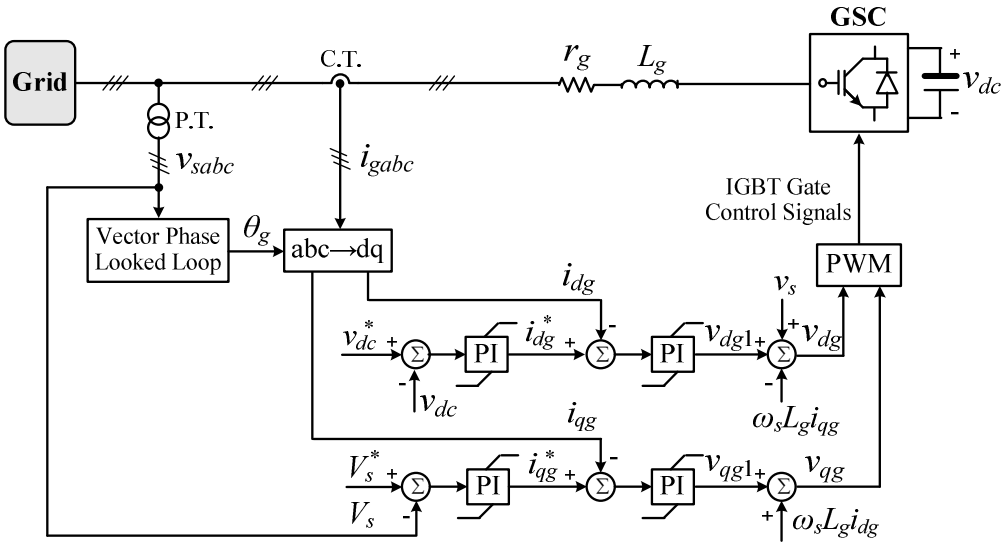


Figure 2.4 Overall FOC control scheme of the GSC.

A significant difference between the RSC and GSC is that the fundamental frequency of the GSC is the grid frequency f_s (typically 50 Hz or 60 Hz), but the RSC is frequently operating at lower fundamental frequencies, i.e., the slip frequency sf_s, where the slip

$$s = \frac{\omega_s - \omega_r}{\omega_s} \tag{2.9}$$

is typically within ±33% [57]. Different fundamental frequencies cause different thermal stress to the RSC and GSC.

2.2 Space Vector Modulation Methods for Multilevel Converters

This section reviews existing SVM methods developed for multilevel converters. The ideas, advantages, and drawbacks of those methods are explained in detail.

The SVM algorithm presented in [39] is based on a 60º coordinate system. When a reference vector is provided in the stationary reference frame (α-β coordinates), this unusual 60º coordinate system requires several matrix transformations, and therefore causes extra computational burden. More critically, [39] does not provide a systematic approach for determining the switching sequences. Some studies [58] [59] attempt to solve this problem by using the phase-disposition PWM. Because of the inherent

drawbacks of the carrier-based method (e.g., carrier waves and selected common-mode voltages are needed), this approach not only increases the complexity, but also undermines the flexibility [38]. Sometimes even the carrier waves are required to be sophisticatedly modified for each switch [59], in order to achieve the optimized switch utilization. This is challenging in real applications, especially when the converter consists of a large number of switches.

The methods in [40] and [41] are basically two different representations of the algorithm in [39]. Both methods avoid the unconventional 60º coordinate system, based on a transformation of the reference vector [60] and a transformed α-β coordinate frame [41], respectively. However, neither of the two methods provides a systematic approach to determining the switching sequences, similar to [39]. Moreover, compared to the algorithm in [39], the following extra complexity emerges in the two methods: 1) the sector location of the reference vector needs to be detected in [40], because different sectors apply different formulas for the switching states and duty cycles; 2) the method in [41] requires more operations when recovering the three-dimensional switching sates from the coordinates in the transformed α-β frame.

In [42], a two-level SVM based scheme is described. It consists of a primary unit and a secondary unit. The primary unit identifies the triangle that encloses the tip of the reference vector, determines a small vector for a virtual two-level converter, and then obtains the duty cycles based on a two-level SVM. An advantage of this method is that the calculation of duty cycles is independent of the level number. On the contrary, the secondary unit requires a pre-stored switching sequence mapping table to determine the switching states and sequences, which is significantly influenced by the level number of the converter. Since the number of available switching sequences increases rapidly with the higher number of levels, more memory will be needed and a slower mapping speed will be achieved when this method is applied to higher level converters. In fact, the

memory required to store the switching states for an n-level converter is $3n^3(n\text{-}1)/8$ bytes [42].

Another method based on the concept of two-level SVM is introduced in [43]. To detect the center of a two-level hexagon that contains the tip of the reference vector, a so called "distance term" needs to be calculated and compared for each vector on the inner side of a particular layer (i.e., the hexagonal ring where the reference vector is located). This iterative operation will lead to considerable computation time when the level number of the converter is large, because more vectors exist in the space vector diagram. An extra two-phase to three-phase conversion is also required to identify the particular layer, since most control schemes give a reference vector in two-dimensional coordinates. Moreover, in this method some switching states and sequences that are actually suitable for the reference vector are ignored, which causes the method to not provide optimal switching waveforms for every operation condition.

The general n-level scheme in [44], for the first time, proposes a systematic approach to easily determine all the available switching sequences. The basic idea is virtually reducing the level number of the converter, until a two-level hexagon that encircles the vertex of the reference vector is identified; the shifting of vectors is represented by adjusting the switching states of the corresponding phase. Finally, this scheme calculates the duty cycles simply as if for a two-level SVM, and generates all the available switching states and sequences based on two simple and general mappings. No lookup table or coordinate transformation is needed. However, the detection of the two-level hexagon is achieved by determining a set of nested hexagons, which is dependent on the level number and requires iterative calculations. These iterative calculations reduce the computational efficiency of the scheme when the level number is large. Moreover, because of the encoding (which causes complexity and extra memory consumption in real-time implementation) needed for the four switching states and the respective duty cycles in each switching sequence, the proposed approach of generating switching

sequences is still relatively more complicated than the other two types of modulation methods.

In summary, there exist non-ignorable drawbacks in each of the earlier SVM methods [39]-[44]. Table 2.1 summarizes the comparison between earlier SVM and the other two modulation methods, in terms of flexibility and ease of implementation [38]. Because of its complicated implementation, SVM is less frequently adopted for large level numbers (such as MMC and HVDC applications [24] [61]), in spite of its significant flexibility. Furthermore, none of the earlier SVM methods [39]-[44] are capable of dealing with increasingly employed multiphase multilevel converters [62] [63]. For example, the 60º coordinate system in [39] is specific to three-phase systems, and cannot be extended to other multiphase applications. A further simplified and generalized SVM scheme is therefore needed.

Table 2.1 Comparison of Earlier SVM and the Other Two Modulation Methods

	Comparison
Flexibility	SVM > nearest-level modulation > carrier-based modulation
Ease of implementation	nearest-level modulation > carrier-based modulation > SVM

2.3 Power Loss Balancing Schemes for Three-Level ANPC Converters

This section introduces the background of deriving the ANPC technique from the original neutral point clamped (NPC) converter, and reviews existing power loss balancing schemes reported for the three-level ANPC converter.

2.3.1 Derivation of the ANPC Converter

Since its emergence in the early 1980s [15], the three-level NPC converter shown in Figure 1.4(a) has attracted wide research attention, especially in high-power medium-voltage applications [45] [64]. One increasing market of the NPC converter is the application in wind energy conversion systems (WECSs) [10] [65]. Nowadays, the

largest wind turbine reaches a power rating of 8 MW [7], which is challenging for the existing two-level converter technology because of the voltage/current limits of power devices. The NPC converter offers a simple approach to reduce the voltage stress on the power devices, and therefore extends the voltage and power ranges of the two-level topology. Compared with two-level converters, the NPC topology demonstrates various other advantages, such as lower harmonics, longer device lifetime, and smaller instantaneous rate of voltage change (dv/dt) [14].

However, a major drawback of the NPC converter is the unequal power loss distribution among the semiconductors [46]. The unbalanced power losses cause unequal thermal stress among the semiconductors, and both the power rating and lifetime of the converter are limited by the most stressed devices. In the applications of WECSs, the converters frequently operate at low fundamental frequencies, which further aggravate the power loss and junction temperature unbalance. For example, typically the frequency (i.e., slip frequency) of the rotor side converter in a DFIG- based WECS is within ±33% of the synchronous frequency [57]. A direct consequence of a low fundamental frequency is that the most stressed power devices are continuously heated up for longer periods than at the synchronous frequency; junction temperature ripples are increased, and the power devices' lifetimes are compromised.

To overcome the loss unbalance problem of the NPC converter, the ANPC (active NPC) technique shown in Figure 2.5 was introduced in 2001 [47]. It replaces the clamp diodes in the NPC converter with active/controllable power devices, thus offering more flexibility for loss balancing control. Table 2.2 summarizes all the available switching states of the three-level ANPC converter, where the states "1" and "0" represent the ON and OFF states of a switch, respectively. Compared with the original NPC topology (which has only one "0" switching state to turn on the neutral clamping path), the ANPC converter offers nine "0" switching states ($0U_1$~$0U_4$, 0UL, and $0L_1$~$0L_4$) to implement the neutral point clamping.

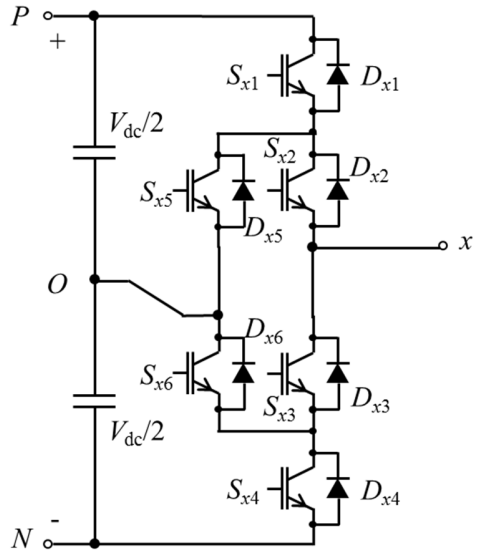


Figure 2.5 Single-phase circuit diagram of the ANPC converter.

Table 2.2 Available Switching States of the Three-Level ANPC Converter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}
P	1	1	0	0	0	1
$0U_1$	0	1	0	0	1	0
$0U_2$	0	1	0	1	1	0
$0U_3$	0	1	1	0	1	0
$0U_4$	0	1	0	0	1	1
0UL	0	1	1	0	1	1
$0L_1$	0	0	1	0	0	1
$0L_2$	1	0	1	0	0	1
$0L_3$	0	1	1	0	0	1
$0L_4$	0	0	1	0	1	1
N	0	0	1	1	1	0

2.3.2 Power Loss Balancing Methods for the ANPC Converter

Some pulse width modulation (PWM) methods [66]-[69] have been investigated to redistribute the power losses, but the solution is still at an early stage, considering the flexibility of selecting redundant switching states that the ANPC topology provides.

The method in [66] depends on device temperature feedback and online temperature calculation using the devices' thermal model. This process is very complicated and introduces a heavy computational burden. In addition, the temperature sensors and parameters of the devices for the thermal model have to be very precise (which is not

easy in real applications) in order to obtain accurate control performance. Therefore, this method is not suited to real-time implementation.

The methods introduced in [67] and [68] are based on revising the switching patterns of each phase leg of the ANPC converter. However, [67] only works for a very narrow range of the power factor (around 1), while in [68] only one "0" switching state is used and therefore significant flexibility is lost. Both [67] and [68] cannot maximally balance the devices' power losses and thermal stress.

Among the earlier modulation methods, the doubled frequency PWM (DF-PWM) [69] is of particular interest because it naturally doubles the apparent switching frequency (the equivalent switching frequency observed from the output voltage waveforms). However, it has been demonstrated [48] that in many cases, this modulation method for the ANPC converter only marginally relieves the loss unbalance problem.

Chapter 5 explains the DF-PWM method in more detail, and proposes an improved modulation method for power loss balancing of the ANPC converter.

2.4 Modulation and Control of the Modular Multilevel Converter

The control of the MMC, including capacitor voltage balancing and circulating current suppression, is typically achieved at the modulation stage. This section reviews existing modulation and control methods for the MMC.

2.4.1 Modulation Methods

Low-frequency modulation methods, such as the selective harmonic elimination [70] and the nearest level control [71] [72], represent one control approach for the MMC. It is an advantage of these modulation methods that the power losses of the MMC are smaller than using modulation methods at high switching frequencies. However, large submodule (SM) capacitors are usually required by these modulation methods in order to reduce the capacitor voltage ripples. Computation of many switching angles also adds complexity to some of the methods [70].

Several high-frequency pulse width modulation (PWM) methods have been applied to the MMC, and most of them can be classified into two categories, i.e., the carrier-based modulation (including the phase-shifted PWM [27]-[30] [72] [73] and the phase-disposition PWM [32] [33]) and the nearest-level modulation (NLM) [34]-[38] methods. The phase-shifted PWM based control is achieved by individually modifying the modulation signals for each SM. When the MMC consists of a large number of SMs, the computational burden and complexity of the phase-shifted PWM based control significantly increase. On the other hand, the NLM and phase-disposition PWM methods only require controllers for each entire arm of the MMC. This offers an advantageous feature for the MMC with a large number of SMs. Furthermore, the NLM is easier to implement than the phase-disposition PWM, because no carrier waves or associated modifications are needed.

Compared with the aforementioned modulation methods, the space vector modulation (SVM) provides more flexibility to optimize the performance of multilevel converters [38] [44] [75]. However, few SVM strategies have been reported for the MMC at this time. The obstacle for applying SVM to the MMC is the difficulty caused by the largely increased number of switching states that accompany the larger number of levels. In [61], a SVM method with control of capacitor voltages and circulating currents for the MMC is presented, but its implementation requires further simplification. A dual SVM scheme is introduced in [76] for the MMC; however, the required two SVM schemes increase both computational burden and complexity of the method. In addition, no control of capacitor voltages (except the sorting approach) and circulating currents is implemented in [76].

2.4.2 Capacitor Voltage Balancing

A well-known capacitor voltage balancing method of the MMC is the so-called “sorting method” [32] [36], which selects the ON-state SMs of each arm of the MMC according to the direction of the arm current. However, the sorting method can only

balance the capacitor voltages of the SMs within one arm, and therefore the SM capacitor voltages in different arms may diverge. As a result, the "sorting method" is usually accompanied by other capacitor voltage control loops/strategies.

Since the SM capacitor voltages are mutually coupled with the circulating current within the same phase leg of the MMC, one common approach of capacitor voltage balancing is to regulate the corresponding circulating current. A reference value of the circulating current (with injection of specific harmonics) can either be generated based on the steady-state operating conditions of the MMC [77], or be obtained from instantaneous information (SM capacitor voltages, output currents, etc.) of the MMC through some capacitor voltage balancing control loops [27] [35] [61].

Another approach of capacitor voltage balancing (as well as circulating current suppression) is using the so-called "model predictive control (MPC)" [78]-[80], which predicts the capacitor voltages and circulating currents based on the model of the MMC. This method requires accurate information (parameters, operating conditions, etc.) of the MMC in order for the model to function well. In addition, an imminent objective of this method is to reduce the computational burden when the MMC consists of a large number of SMs.

2.4.3 Circulating Current Suppression

In order to reduce the power losses and maintain the ratings of the MMC, the harmonics (mainly the 2nd-order) in the circulating current have to be eliminated. Typically two methods have been reported.

One method is based on resonant [81] or repetitive controllers [73], which eliminate the harmonic components of the circulating current at the resonant frequencies. In order to reduce the sensitivity to the frequency deviation around the resonant frequency, non-ideal resonant controllers [82] with a bandwidth (a margin of the resonant frequency) can be adopted.

Based on the synchronous reference frame, the other method applies proportional-integral (PI) controllers instead of resonant controllers to eliminate specific harmonics of the circulating currents [28]. This approach is not as flexible as the other one because a synchronous reference frame (coordinate transformation) has to be carried out for each harmonic component that is required to eliminate.

2.5 Chapter Summary

This chapter has presented a comprehensive literature review on existing methods and techniques related to this dissertation work. First, the typical modelling and control methods for wind turbines and doubly-fed induction generators (DFIGs) are summarized. This facilitates the development of control schemes for power electronic converters in DFIG-based wind energy generation systems. Next, the existing space vector modulation (SVM) methods for multilevel converters are introduced. Then, the existing power loss balancing schemes for three-level active neutral-point-clamped (ANPC) converters are reviewed. Finally, the existing modulation and control methods for the modular multilevel converter (MMC) are discussed.

Based on this literature review, the rest of this dissertation proposes new methods to solve the remaining problems. The next chapter investigates the inherent relationship between the SVM and the nearest-level modulation methods despite their apparent differences, in order to simplify the implementation of the SVM method.

CHAPTER 3 SPACE-VECTOR VERSUS NEAREST-LEVEL PULSE WIDTH MODULATION FOR MULTILEVEL CONVERTERS

As compared in Chapters 1 and 2 with the other two widely used pulse width modulation methods (carrier-based modulation and nearest-level modulation) for multilevel converters, space vector modulation (SVM) conveniently provides more flexibility (i.e., redundant switching sequences and adjustable duty cycles) to optimize switching waveforms, but requires more complicated implementation.

This chapter studies the inherent relationship between the SVM and the nearest-level modulation methods despite their apparent differences, in order to simplify the implementation of the SVM method. The nearest-level modulation method directly controls the voltage of each phase, while the SVM method simultaneously deals with all phases. It is demonstrated in this chapter that the two modulation methods are functionally equivalent: with proper common-mode voltage injections, the nearest-level modulation method is equivalent to the SVM method; by selecting the appropriate redundant switching sequences and the corresponding duty cycles, the SVM method is equivalent to the nearest-level modulation method. Nevertheless, the SVM method can conveniently provide more flexibility of optimizing the switching patterns, without the need of designing sophisticated common-mode voltages. An efficient and flexible modulation method for any multiphase multilevel converter is therefore proposed, which combines the advantages of the nearest-level modulation and the SVM methods, i.e., both with less computational burden and high flexibility of optimizing the output waveforms. Simulation and experimental results validate the analysis.

3.1 Principle of SVM and Nearest-Level Modulation

3.1.1 Space Vector Modulation

The SVM method proposed in [44], as illustrated in Figure 3.1, is considered as an example to demonstrate the principle of space vector modulation methods for *n*-level converters. Though other SVM methods can be realized by different approaches, they obey the same principle, as introduced below.

Figure 3.1(a) shows the space vector diagram of a five-level converter and a reference vector $\boldsymbol{V}_{\text{ref}}$ located inside it. Increasing the level number of the converter by one always forms an additional hexagonal ring of equilateral triangles, which surrounds the outermost hexagon H_0. In order to synthesize the reference vector $\boldsymbol{V}_{\text{ref}}$, it is the task of an SVM method to detect the modulation triangle $\Delta P_1P_2P_3$ (i.e., the nearest three vectors $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$), to determine the switching sequence (sequence of the nearest three vectors), and to calculate the duty cycles (needed durations) of the nearest three vectors.

The modulation triangle $\Delta P_1P_2P_3$ is detected in [44] by determining a set of nested hexagons (i.e., H_1, H_2, and H_3) that respectively correspond to a specific converter level number. After the equivalent two-level hexagon H_3 that encloses the tip of the reference vector $\boldsymbol{V}_{\text{ref}}$ is detected, the origin of the reference vector is shifted to the center of the two-level hexagon H_3 and a remainder vector $\boldsymbol{V}_{\text{ref}}'$ is generated. Based on the remainder vector $\boldsymbol{V}_{\text{ref}}'$, the switching sequences [e.g., 142 → 141 → 041 → 031 in Figure 1(b)] and duty cycles are obtained in the same way as for a two-level converter, as shown in Figure 3.1(b) and (c). A more detailed explanation for the symbols in Figure 3.1 can be found in [44].

For a three-phase *n*-level converter, an output voltage space vector that represents the switching states of all the phases is defined [44] as

$$\boldsymbol{V}_{out} = V_{dc} \cdot (S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi}) \tag{3.1}$$

where V_{dc} is the dc-link voltage of the converter; S_a, S_b, and S_c (S_a, S_b, S_c=0, 1, …n-1) are the switching states of phases A, B, and C, respectively. Accordingly, the voltage of phase h (h=A, B, or C) relative to the negative terminal of the dc-link is $S_h \cdot V_{dc}/(n\text{-}1)$. The definition in (3.1) makes the side length of each modulation triangle (e.g., $\Delta P_1P_2P_3$) in the space vector diagram to be V_{dc}.

Corresponding to (3.1), the reference vector $\boldsymbol{V}_{ref}$ of the n-level converter is generated [44] as

$$\boldsymbol{V}_{ref} = (n-1)\left(V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi}\right) \tag{3.2}$$

where V_a^*, V_b^*, and V_c^* are respectively the reference voltages of phases A, B, and C relative to the negative terminal of the dc-link. The nearest three vectors $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$ [calculated from (3.1)] synthesize the reference vector as follows [39]

$$\boldsymbol{V}_{ref} = D_1 \cdot \boldsymbol{OP}_1 + D_2 \cdot \boldsymbol{OP}_2 + D_3 \cdot \boldsymbol{OP}_3 \tag{3.3}$$

where D_1, D_2, and D_3 are the duty cycles of $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$, respectively.

The SVM method simultaneously deals with all the phases (i.e., directly works on the line-to-line voltages), as shown in (3.2). If a carrier-based or nearest-level modulation method is adopted, the reference voltage V_h^* of phase h (h=A, B, or C) is

$$V_a^* = m \cdot \frac{V_{dc}}{\sqrt{3}} \cos(\theta) + V_{com} \tag{3.4a}$$

$$V_b^* = m \cdot \frac{V_{dc}}{\sqrt{3}} \cos\left(\theta - \frac{2}{3}\pi\right) + V_{com} \tag{3.4b}$$

$$V_c^* = m \cdot \frac{V_{dc}}{\sqrt{3}} \cos\left(\theta + \frac{2}{3}\pi\right) + V_{com} \tag{3.4c}$$

where m is the modulation index; θ is the phase angle of the phase A voltage; V_{com} is the common-mode voltage and can be constant or time-variant (such as third-order harmonics), depending on the application [36] [58].

Substituting (3.4) into (3.2) rewrites the reference vector $\boldsymbol{V}_{ref}$ as

$$\boldsymbol{V}_{ref} = (n-1) \cdot \left(m \cdot \frac{\sqrt{3}}{2} V_{dc} \cdot e^{j\theta}\right) \tag{3.5}$$

Equations (3.4) and (3.5) indicate that the common-mode voltage V_{com} has no influence on the reference vector $\boldsymbol{V}_{ref}$ or the line-to-line voltages. Therefore, compared to the other two types of modulation methods, the SVM method can be more flexibly implemented in any modulation range without the need of sophisticated reference voltage signals.

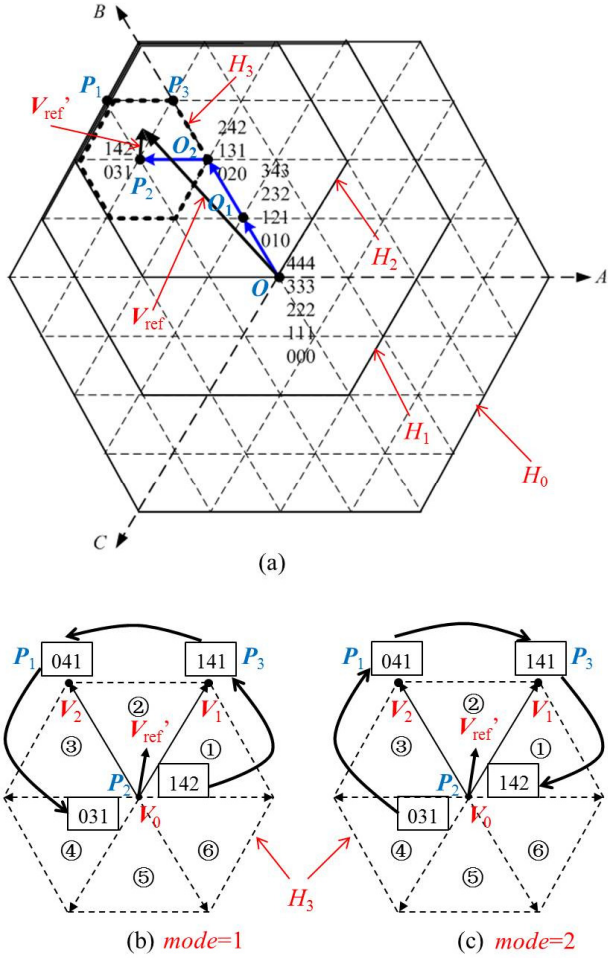


Figure 3.1 SVM method proposed in [44]: (a) detecting the modulation triangle; (b)-(c) two switching sequence modes.

3.1.2 Nearest-Level Modulation

Unlike the SVM methods, the nearest-level modulation method [83]-[37] directly controls the phase voltages of the converter and allows the line-to-line voltages to be developed implicitly. Figure 3.2 illustrates the general approach of the nearest-level modulation method. For each switching cycle, the switching state S_h of phase h (h=A, B,

or C) in (3.1) has two values, i.e., K_h and K_h+1, and the corresponding duty cycles are respectively 1-D_h and D_h. The reference voltage of each phase in (3.4) is approximated by the two nearest voltage levels $K_h V_{dc}/(n\text{-}1)$ and $(K_h\text{+}1)V_{dc}/(n\text{-}1)$, based on [36]

$$V_h^* = (1 - D_h) \cdot \frac{K_h V_{dc}}{n-1} + D_h \cdot \frac{(K_h+1)V_{dc}}{n-1} = (K_h + D_h)V_{dc}/(n-1) \tag{3.6}$$

The switching states and duty cycles of each phase are consequently obtained [36] as

$$K_h = \text{int}\left(\frac{V_h^*}{V_{dc}/(n-1)}\right) \tag{3.7}$$

$$D_h = \frac{V_h^*}{V_{dc}/(n-1)} - K_h \tag{3.8}$$

where int(x) means the integer part of x. Considering the definition of the switching state, the reference voltage of phase h (h=A, B, or C) should be within the following range

$$0 \le V_h^* \le V_{dc} \tag{3.9}$$

which implies that if the common-mode voltage is a constant (e.g., $V_{com} = m \cdot V_{dc}/\sqrt{3}$), the modulation index m should be less than 0.866. However, there is no such restriction for the SVM methods.

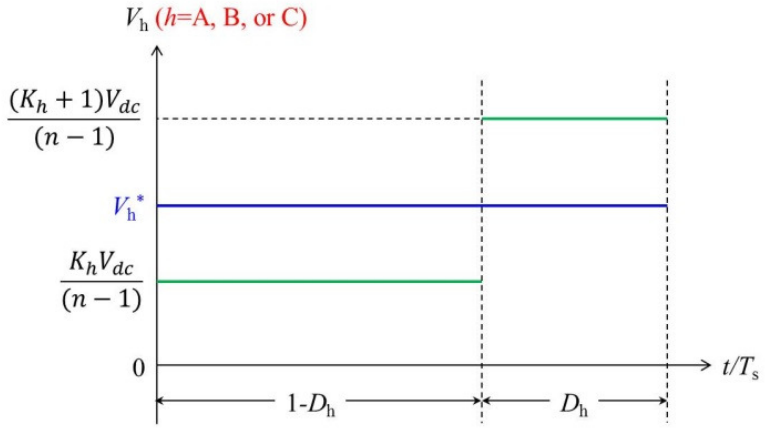


Figure 3.2 The reference voltage $\boldsymbol{V}_{\mathbf{h}}^*$ and the corresponding output phase voltage V_h (h=A, B, or C) during a switching cycle T_s for the nearest-level modulation method.

It is shown by (3.6)-(3.9) that for the nearest-level modulation method, the switching states and the corresponding duty cycles for each phase are influenced by the common-mode voltage V_{com}, and thus sometimes dedicated reference voltages are required in order

to achieve a better performance, such as higher modulation indexes [36]. This is discussed in more detail in the next sections. Substituting (3.4) into (3.9) gives the following feasible region for the common-mode voltage

$$-\min(V_{a1}, V_{b1}, V_{c1}) \le V_{com} \le V_{dc} - \max(V_{a1}, V_{b1}, V_{c1}) \tag{3.10}$$

where $\min(V_{a1}, V_{b1}, V_{c1})$ and $\max(V_{a1}, V_{b1}, V_{c1})$ respectively mean the minimum and maximum value among V_{a1}, V_{b1}, and V_{c1}; and V_{a1}, V_{b1}, and V_{c1} respectively represent the fundamental-frequency components of V_h^* (h=A, B, or C) as

$$V_{a1} = m \cdot \frac{V_{dc}}{\sqrt{3}} \cos(\theta) \tag{3.11a}$$

$$V_{b1} = m \cdot \frac{V_{dc}}{\sqrt{3}} \cos\left(\theta - \frac{2}{3}\pi\right) \tag{3.11b}$$

$$V_{c1} = m \cdot \frac{V_{dc}}{\sqrt{3}} \cos\left(\theta + \frac{2}{3}\pi\right) \tag{3.11c}$$

3.1.3 Apparent Difference between SVM and Nearest-Level Modulation

Illustrated in Figure 3.3 are the switching sequence and the corresponding duty cycles of the SVM and the nearest-level modulation methods. For the SVM method, the continuous switching sequence pattern (i.e., all the phases are modulated during a switching cycle) is considered as an example in the following analysis. The discontinuous SVM patterns [58] (i.e., eliminating either the first or last switching state in each switching sequence) can be analyzed in a similar way.

As shown in Figure 3.3(a), for the SVM method, four switching states compose a switching sequence and the first and last switching states are redundant switching states. For example, the switching sequences shown in Figure 1 are 142 → 141 → 041 → 031 for *mode*=1 (descending mode) and 031 → 041 → 141 → 142 for *mode*=2 (ascending mode) [44]. Since the redundant switching states (e.g., 142 and 031) produce the same voltage space vector, their duty cycles (i.e., d_{01} and d_{02}) can be freely adjusted as long as the summation is a constant [44] [58]:

$$d_{01} + d_{02} = 1 - d_1 - d_2, \quad d_{01} \ge 0 \text{ and } d_{02} \ge 0 \tag{3.12}$$

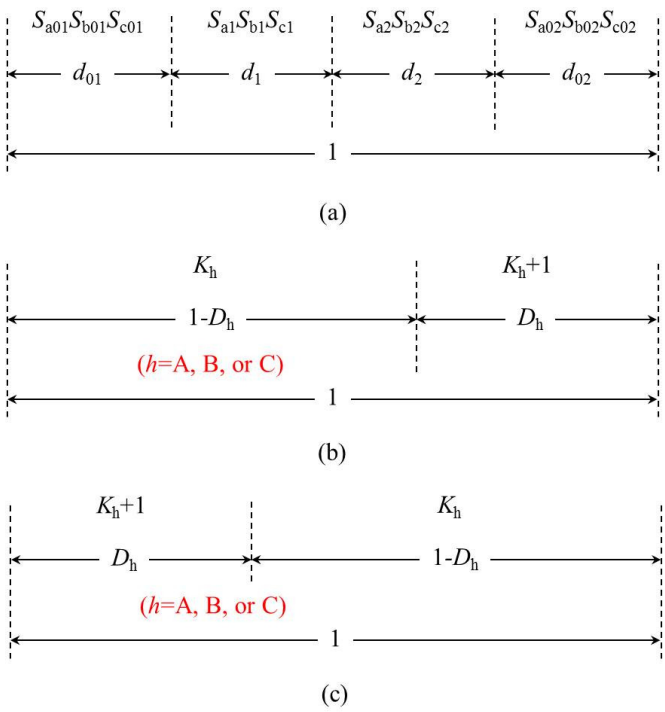


Figure 3.3 The switching states and the corresponding duty cycles of the modulation methods: (a) SVM; (b) nearest-level modulation in ascending mode; (c) nearest-level modulation in descending mode.

When the reference vector is located in the low modulation regions, e.g., $m < (n\text{-}2)/(n\text{-}1)$ in (3.5), for any switching sequence shown in Figure 3.3(a), a set of redundant switching sequences can be generated by the SVM method [44] [58] [83] as

$$\begin{bmatrix} S_{a01}+k \\ S_{b01}+k \\ S_{c01}+k \end{bmatrix} \rightarrow \begin{bmatrix} S_{a1}+k \\ S_{b1}+k \\ S_{c1}+k \end{bmatrix} \rightarrow \begin{bmatrix} S_{a2}+k \\ S_{b2}+k \\ S_{c2}+k \end{bmatrix} \rightarrow \begin{bmatrix} S_{a02}+k \\ S_{b02}+k \\ S_{c02}+k \end{bmatrix} \tag{3.13}$$

where k is an integer and

$$-\min(S_{a01}, S_{b01}, S_{c01}) \le k \le n-2-\max(S_{a01}, S_{b01}, S_{c01}), \text{ if } S_{a02} > S_{a01} \tag{3.14a}$$

$$1-\min(S_{a01}, S_{b01}, S_{c01}) \le k \le n-1-\max(S_{a01}, S_{b01}, S_{c01}), \text{ if } S_{a02} < S_{a01} \tag{3.14b}$$

where $\min(S_{a01}, S_{b01}, S_{c01})$ and $\max(S_{a01}, S_{b01}, S_{c01})$ are respectively the minimum and maximum values among S_{a01}, S_{b01}, and S_{c01}.

The nearest-level modulation method also generally arranges the switching sequences in two modes, i.e., the ascending and descending modes, as respectively shown in Figure 3.3(b) and (c). For every switching cycle, the switching states of each phase are increasing (from K_h to K_h+1) in the ascending mode while decreasing (from K_h+1 to K_h) in the descending mode. Note that in order to reduce the harmonics in line-to-line voltages, all the phases should adopt the same switching sequence mode (ascending or descending) for each switching cycle.

Through the above description, no obvious relationship between the SVM and the nearest-level modulation methods can be observed. It also seems that compared to the SVM method, two degrees of freedom, i.e., the redundant switching sequences and the adjustable duty cycles, are lost in the nearest-level modulation method. The essential reason for this phenomenon is discussed below in detail, together with demonstrating the equivalence of the two modulation methods.

3.2 Equivalence of SVM to Nearest-Level Modulation

The SVM method can equivalently realize the switching sequences and the duty cycles generated by the nearest-level modulation method, as demonstrated below. Now the switching states K_h and K_h+1 (h=A, B, or C) and the corresponding duty cycles 1-D_h and D_h (h=A, B, or C) shown in Figure 3.3(b) and (c) are already generated by the nearest-level modulation method based on (3.6)-(3.9), for any valid common-mode voltage. Without loss of generality, assume

$$D_c \leq D_a \leq D_b \tag{3.15}$$

According to (3.15), the switching states and the corresponding duty cycles for the three phases, generated by the nearest-level modulation method, can be arranged in the following two ways to construct two switching sequences:

$$\begin{matrix} \begin{bmatrix} K_a+1 \\ K_b+1 \\ K_c+1 \end{bmatrix} & \rightarrow & \begin{bmatrix} K_a+1 \\ K_b+1 \\ K_c \end{bmatrix} & \rightarrow & \begin{bmatrix} K_a \\ K_b+1 \\ K_c \end{bmatrix} & \rightarrow & \begin{bmatrix} K_a \\ K_b \\ K_c \end{bmatrix} \\ \Updownarrow & & \Updownarrow & & \Updownarrow & & \Updownarrow \\ D_c & & D_a - D_c & & D_b - D_a & & 1 - D_b \end{matrix} \tag{3.16a}$$

$$\begin{matrix} \begin{bmatrix} K_a \\ K_b \\ K_c \end{bmatrix} & \rightarrow & \begin{bmatrix} K_a \\ K_b+1 \\ K_c \end{bmatrix} & \rightarrow & \begin{bmatrix} K_a+1 \\ K_b+1 \\ K_c \end{bmatrix} & \rightarrow & \begin{bmatrix} K_a+1 \\ K_b+1 \\ K_c+1 \end{bmatrix} \\ \Updownarrow & & \Updownarrow & & \Updownarrow & & \Updownarrow \\ 1 - D_b & & D_b - D_a & & D_a - D_c & & D_c \end{matrix} \tag{3.16b}$$

which are equivalent to the descending and ascending switching sequences shown in Figure 3.3(c) and (b), respectively. For example, Figure 3.4 illustrates the switching sequence obtained from (3.16b); reversing it gives the sequence in (3.16a).

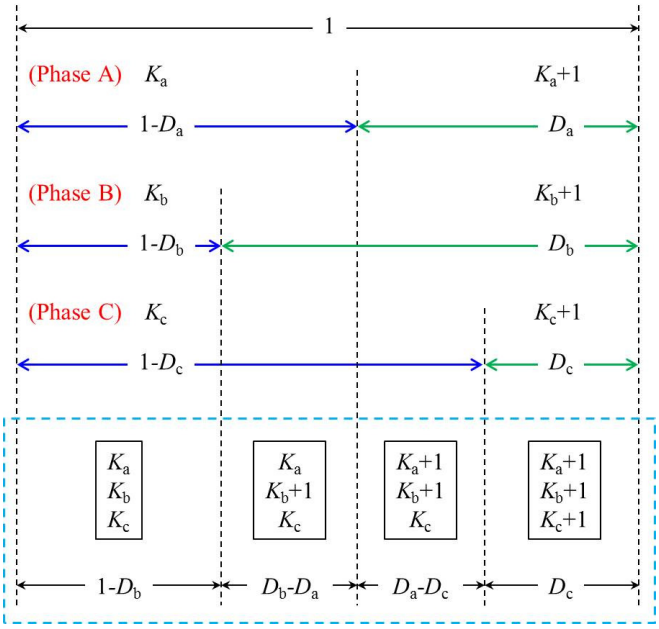


Figure 3.4 The switching sequence shown in (3.16b).

Each switching sequence in (3.16) can be represented as the sequence shown in Figure 3.3(a), but is it a result of the SVM method? To answer this question, (3.6) is re-written as

$$V_a^* = (d_{01}S_{a01} + d_1S_{a1} + d_2S_{a2} + d_{02}S_{a02})V_{dc}/(n-1) \tag{3.17a}$$

$$V_b^* = (d_{01}S_{b01} + d_1S_{b1} + d_2S_{b2} + d_{02}S_{b02})V_{dc}/(n-1) \tag{3.17b}$$

$$V_c^* = (d_{01}S_{c01} + d_1S_{c1} + d_2S_{c2} + d_{02}S_{c02})V_{dc}/(n-1) \tag{3.17c}$$

which by respectively multiplying (3.17b) with $e^{j\frac{2}{3}\pi}$ and (3.17c) with $e^{j\frac{4}{3}\pi}$, leads to the following equation

$$\begin{aligned}(n-1)\left(V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi}\right) &= d_{01}V_{dc}\left(S_{a01} + S_{b01} \cdot e^{j\frac{2}{3}\pi} + S_{c01} \cdot e^{j\frac{4}{3}\pi}\right) \\ +d_1V_{dc}\left(S_{a1} + S_{b1} \cdot e^{j\frac{2}{3}\pi} + S_{c1} \cdot e^{j\frac{4}{3}\pi}\right) &+ d_2V_{dc}\left(S_{a2} + S_{b2} \cdot e^{j\frac{2}{3}\pi} + S_{c2} \cdot e^{j\frac{4}{3}\pi}\right) \\ +d_{02}V_{dc}\left(S_{a02} + S_{b02} \cdot e^{j\frac{2}{3}\pi} + S_{c02} \cdot e^{j\frac{4}{3}\pi}\right)\end{aligned} \tag{3.18}$$

It is seen that (3.17) gives a particular solution to (3.18), by separating the components of each phase.

According to (3.2), the left side of (3.18) is exactly the reference vector $\boldsymbol{V}_{\text{ref}}$. Comparing (3.18) with (3.3) indicates that each switching sequence in (3.16) actually represents a valid switching sequence for the SVM method under the continuous modulation pattern [44] [58]. In (3.16a), the switching state of each phase is descending in the switching sequence, such as the switching sequence 142 → 141 → 041 → 031 for *mode*=1 shown in Figure 3.1. On the contrary, (3.16b) represents an ascending switching sequence, such as the switching sequence 031 → 041 → 141 → 142 for *mode*=2 shown in Figure 3.1.

The above analysis reveals that the result of the nearest-level modulation method is a particular solution to the SVM method. Since for the nearest-level modulation method the common-mode voltage V_{com} can only have a fixed value at any given time, while for the SVM method V_{com} can be any value, the fixed common-mode voltage in (3.17) causes the loss of the two degrees of freedom (i.e., the redundant switching sequences and the adjustable duty cycles). In other words, the common-mode voltage is the essential reason that results in the apparent difference between the SVM and the nearest-level modulation methods.

Note that for a given reference vector, there is only one valid switching sequence for each mode (ascending or descending) if the first switching state is determined [44] [58]. Therefore, the corresponding switching sequence can be selected based on the reference voltage V_{h}^{*} of phase h (h=A, B, or C), or the common-mode voltage, adopted by the nearest-level modulation method. The first switching state of the switching sequence generated by the SVM method is

$$\begin{bmatrix} S_{a01} \\ S_{b01} \\ S_{c01} \end{bmatrix} = \begin{bmatrix} K_a + 1 \\ K_b + 1 \\ K_c + 1 \end{bmatrix}, \quad \text{if (3.16a) is adopted} \tag{3.19a}$$

$$\begin{bmatrix} S_{a01} \\ S_{b01} \\ S_{c01} \end{bmatrix} = \begin{bmatrix} K_a \\ K_b \\ K_c \end{bmatrix}, \quad \text{if (3.16b) is adopted} \tag{3.19b}$$

which consequently yields the remainder vector $\boldsymbol{V}_{\mathrm{ref}}$' in Figure 3.1 for the SVM method [44]. The corresponding duty cycles are

$$\begin{bmatrix} d_{01} \\ d_1 \\ d_2 \\ d_{02} \end{bmatrix} = \begin{bmatrix} D_c \\ D_a - D_c \\ D_b - D_a \\ 1 - D_b \end{bmatrix}, \quad \text{if (3.16a) is adopted} \tag{3.20a}$$

$$\begin{bmatrix} d_{01} \\ d_1 \\ d_2 \\ d_{02} \end{bmatrix} = \begin{bmatrix} 1 - D_b \\ D_b - D_a \\ D_a - D_c \\ D_c \end{bmatrix}, \quad \text{if (3.16b) is adopted} \tag{3.20b}$$

Substituting (3.7) and (3.8) into (3.19) and (3.20) reveals that the effect of adjusting the common-mode voltage in the nearest-level modulation method is equivalently achieved in the SVM method by selecting the proper redundant switching sequence, as in (3.19), and adjusting the duty cycles of the switching states, as in (3.20).

Furthermore, since the duty cycle D_{h} (h=A, B, or C) is the fractional part of $(n-1)V_{\mathrm{h}}^{*}/V_{dc}$, as expressed in (3.8), its adjustment only means a minor change to the common-mode voltage. Large variations of the common-mode voltage are handled in (3.19) by adjusting the redundant switching sequence [i.e., the switching state K_{h} (h=A, B, or C)]. If the adjustment of the common-mode voltage is small, i.e., not cause any

switching state K_h (h=A, B, or C) to change, the duty cycles of the middle two switching states (i.e., d_1 and d_2) in the switching sequence are constant in (3.20). The reason is that the common-mode voltage has the same effect on the duty cycles of all the phases as in (3.8), so the effect is eliminated in the subtraction between the duty cycles of any two phases. Therefore, in this case, only the duty cycles of the first and the last switching states (i.e., d_{01} and d_{02}) need to be adjusted in the SVM method.

The feasible region of the common-mode voltage for different modulation indexes (e.g., m=0.9 and 0.6) of three-phase converters is illustrated in Figure 3.5, where $V_{com,\,max}$ and $V_{com,\,min}$ respectively represents the maximum and minimum limits of the common-mode voltage as in (3.10). The fundamental frequency for Figure 3.5 is 50 Hz. A comparison between Figure 3.5(a) and (b) reveals that the feasible region (encircled by the waveforms of $V_{com,\,max}$ and $V_{com,\,min}$) of the common-mode voltage is larger for m=0.6 than for m=0.9. The area of the feasible region for the common-mode voltage according to a set of different modulation indexes (from 0 to 1) is shown in Figure 3.6, where the area is normalized with respect to A_0 (i.e., the area of the feasible region for the common-mode voltage when m=0). Figures 3.5 and 3.6 demonstrate that when the modulation index decreases, the adjustable range of the common-mode voltage becomes larger and therefore more redundant switching states/sequences need to be generated by the SVM method according to (3.19). This has already been verified for the SVM method in [44] [58].

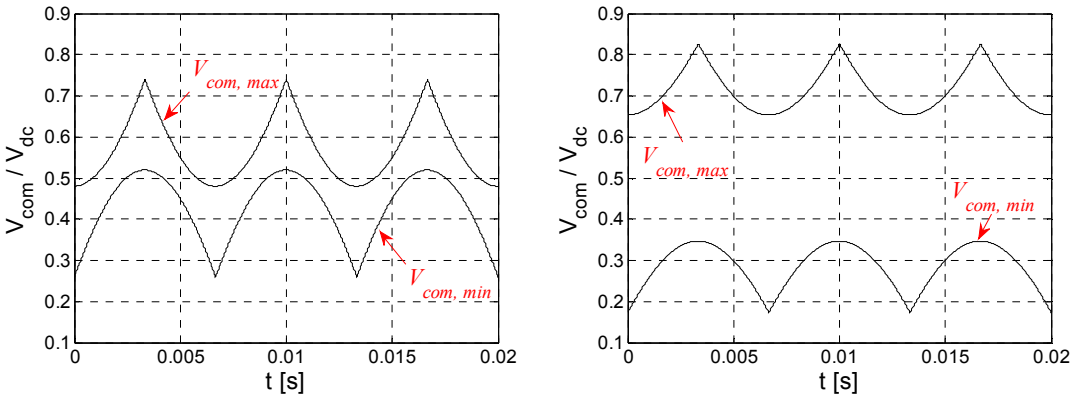


Figure 3.5 Feasible region of the common-mode voltage for different modulation index: (a) m=0.9; (b) m=0.6.

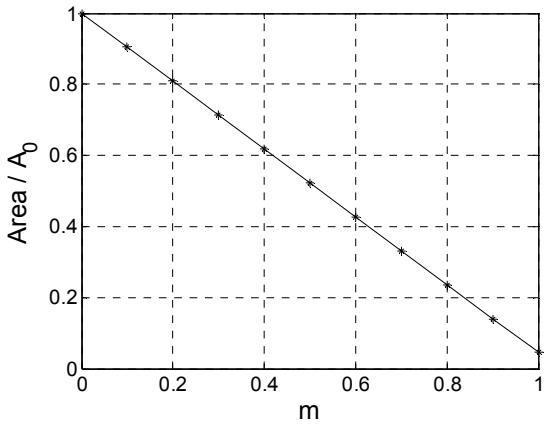


Figure 3.6 Area of the feasible region of the common-mode voltage according to different modulation index (m).

In order to observe the influence of the common-mode voltage on the duty cycles, the switching states in (3.19) are kept unchanged when the common-mode voltage varies. For example, to produce the same switching states with those caused by $V_{\text{com, min}}$, the maximum value of the common-mode voltage is

$$V_{mid} = \min\left\{ \min_{h=a,b,c} \underbrace{\left(\frac{(K_{h,min}+1)V_{dc}}{n-1} - V_{h1} \right)}_{V_{com,h}}, V_{com,max} \right\} \tag{3.21}$$

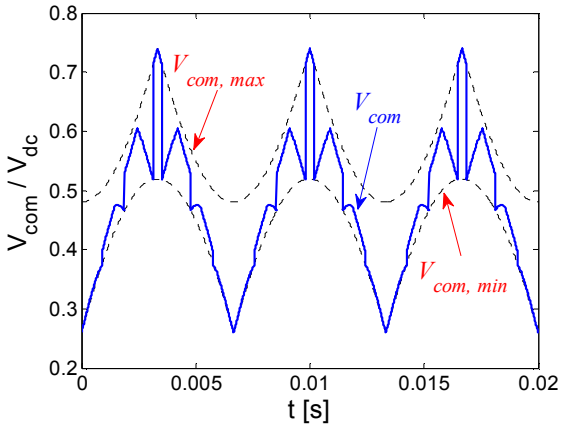
where min(x, y) means the smaller value between x and y; $K_{h,\,min}$ (h=A, B, or C) is the switching state of phase h obtained from (3.7) for $V_{com,\,min}$; V_{h1} is the fundamental-frequency component of phase h reference voltage as shown in (3.11); $V_{com,\,h}$ represents the common-mode voltage required for phase h to change its switching state to $K_{h,\,min}$+1; and [$\min_{h=a,b,c}(V_{com,\,h})$] gives the minimum value among $V_{com,\,h}$ (h=A, B, or C).

Figure 3.7 demonstrates the required duty cycle d_{01} of the first switching state for a five-level converter as an example, when the modulation index is m=0.9, for a common-mode voltage:

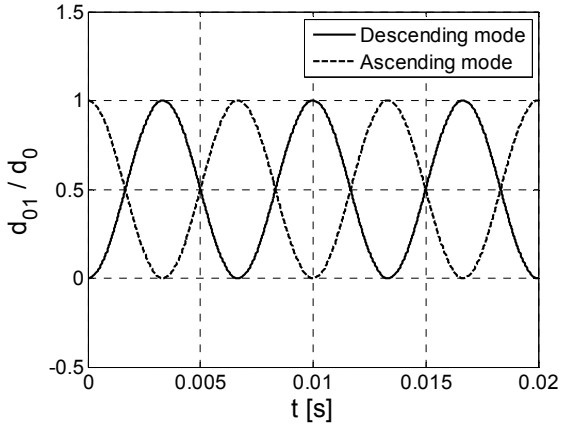
$$V_{com} = 0.5\left(V_{mid} + V_{com,min}\right) - 0.5\left(V_{mid} - V_{com,min}\right) \cdot \cos(3\omega t) \tag{3.22}$$

where ω=2π*50 rad/s is the fundamental angular frequency. As discussed above, the switching state of each phase is always $K_h = K_{h,\,min}$, for any common-mode voltage between $V_{com,\,min}$ and V_{mid}. Therefore, when V_{com}= 0.5(V_{mid} + $V_{com,\,min}$), the duty cycles of the first and the last switching states in each switching sequence are equal, i.e., d_{01}/d_0 is always 0.5 where d_0= d_{01}+d_{02}. The third-order harmonic added to the common-mode voltage in (3.22) causes the normalized duty cycle of the first switching state (i.e., d_{01}/d_0) to vary, as shown in Figure 3.7(b), and the variations for the descending mode (solid line) and the ascending mode (dashed line) are symmetric with respect to d_{01}/d_0= 0.5.

It can be concluded that for any common-mode voltage injection, a nearest-level modulation method can be equivalently realized by an SVM method by selecting the proper redundant switching sequence and duty cycles. The influence of the common-mode voltage is reflected in the SVM by the redundant switching states and their duty cycles in the following two steps: 1) determine the proper switching sequence based on (3.19), called “coarse tuning”; 2) adjust the duty cycles of the first and the last switching states in the switching sequence based on (3.20), called “fine tuning”.



(a)



(b)

Figure 3.7 Influence of the common-mode voltage on the duty cycle of the first switching state in each switching sequence, for modulation index m=0.9 of a five-level converter: (a) the common-mode voltage V_{com} in (3.22); (b) the duty cycle d_{01} of the first switching state in each switching sequence for the two switching sequence modes.

3.3 Equivalence of Nearest-Level Modulation to SVM

On the other hand, it can be shown that any switching sequence and corresponding duty cycles generated by the SVM method can be equivalently obtained from a nearest-level modulation method.

For any optimized switching sequence (with the minimum number of switch transitions in every switching cycle under continuous modulation) generated by the SVM method, as shown in Figure 3.3(a), there are only two successive values S_h and S_h+1

(h=A, B, or C) for the switching state of each phase [44] [58]. For example, the switching state of phase B for the reference vector shown in Figure 3.1 can only have the values of 4 and 3 in the switching sequence 142 → 141 → 041 → 031 for *mode*=1 (descending mode) or 031 → 041 → 141 → 142 for *mode*=2 (ascending mode). Since the first and the last switching states in the switching sequence are redundant switching states, the value of S_h (h=A, B, or C) can be obtained as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} S_{a01} \\ S_{b01} \\ S_{c01} \end{bmatrix}, \quad \text{if } S_{a02} > S_{a01} \text{ (ascending mode)} \tag{3.23a}$$

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} S_{a02} \\ S_{b02} \\ S_{c02} \end{bmatrix}, \quad \text{if } S_{a02} < S_{a01} \text{ (descending mode)} \tag{3.23b}$$

The required reference voltage V_h^* (h=A, B, or C) for the nearest-level modulation method can be generated based on (3.17), and the duty cycles of the same switching state can be combined for each phase. For instance, if the switching sequence is 031 → 041 → 141 → 142 (*mode*=2), the reference voltages for the three phases are respectively

$$\begin{aligned} V_a^* &= (d_{01} + d_1) \cdot \frac{S_a V_{dc}}{n-1} + (d_2 + d_{02}) \cdot \frac{(S_a + 1)V_{dc}}{n-1} \\ &= (S_a + d_a)V_{dc}/(n-1) \end{aligned} \tag{3.24a}$$

$$\begin{aligned} V_b^* &= d_{01} \cdot \frac{S_b V_{dc}}{n-1} + (d_1 + d_2 + d_{02}) \cdot \frac{(S_b + 1)V_{dc}}{n-1} \\ &= (S_b + d_b)V_{dc}/(n-1) \end{aligned} \tag{3.24b}$$

$$\begin{aligned} V_c^* &= (d_{01} + d_1 + d_2) \cdot \frac{S_c V_{dc}}{n-1} + d_{02} \cdot \frac{(S_c + 1)V_{dc}}{n-1} \\ &= (S_c + d_c)V_{dc}/(n-1) \end{aligned} \tag{3.24c}$$

where $[S_a, S_b, S_c]^T = [0, 3, 1]^T$, and

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_2 + d_{02} \\ d_1 + d_2 + d_{02} \\ d_{02} \end{bmatrix} \tag{3.25}$$

For any other continuous switching sequence, an equation similar to (3.24) can be generated. In fact, (3.23) and (3.25) are respectively the reverse processing of (3.19) and (3.20).

For a valid switching sequence of an n-level converter generated by the SVM method, $0 \leq S_h \leq n-1$ and $0 \leq S_h+1 \leq n-1$ (h=A, B, or C), so the reference voltages V_h^* (h=A, B, or C) for the nearest-level modulation method obtained from (3.17) or (3.24) meet the constraint in (3.9). Therefore, these reference voltages can be applied to the nearest-level modulation method. Based on the switching states in (3.23) and the duty cycles in (3.25) for these reference voltages, the switching sequence of the SVM method can be equivalently produced by the nearest-level modulation method according to (3.16).

The corresponding common-mode voltage V_{com} is

$$V_{com} = \frac{1}{3}(V_a^* + V_b^* + V_c^*)$$

$$= \frac{1}{3}\left\{\sum_{h=a,b,c}(d_{01}S_{h01} + d_1S_{h1} + d_2S_{h2} + d_{02}S_{h02})\right\} \cdot V_{dc}/(n-1) \quad (3.26)$$

For example, for the switching sequence 031 → 041 → 141 → 142 (*mode*=2), substituting (3.24) into (3.26) yields

$$V_{com} = \frac{1}{3}(S_a + S_b + S_c + d_1 + 2d_2 + 3d_{02})V_{dc}/(n-1) \quad (3.27)$$

The duty cycles (i.e., d_{01} and d_{02}) of the first and the last switching states in the switching sequence can be freely adjusted as long as the summation is a constant, as shown in (3.12). When the reference vector is located in the low modulation regions, as expressed in (3.13), a set of redundant switching sequences can be generated by the SVM method. According to (3.26) and (3.27), the two degrees of freedom (i.e., the redundant switching sequences and the adjustable duty cycles) provided by the SVM method can be equivalently achieved in the nearest-level modulation method by adjusting the common-mode voltage. For a given reference vector, the duty cycles (i.e., d_1 and d_2) of the middle two switching states in each switching sequence are constant [44] [58], so the adjustment for the common-mode voltage in (3.26) is

$$\Delta V_{com} = (k + \Delta d_{02}) \cdot V_{dc}/(n-1), \quad \text{if } S_{a02} > S_{a01} \text{ (i.e., ascending mode)} \tag{3.28a}$$

$$\Delta V_{com} = (k - \Delta d_{02}) \cdot V_{dc}/(n-1), \quad \text{if } S_{a02} < S_{a01} \text{ (i.e., descending mode)} \tag{3.28b}$$

where k denotes the change of the redundant switching states as in (3.13), and Δd_{02} represents the adjustment for the duty cycle of the last switching state. For example, (3.28a) shows the required adjustment for the common-mode voltage in (3.27).

Figure 3.8 illustrates the relationship between the common-mode voltage and the duty cycle of the last switching state for a five-level converter when the modulation index is m=0.9, in ascending switching sequence mode. $V_{\text{com, max}}$ and $V_{\text{com, min}}$ are respectively the maximum and minimum limits of the common-mode voltage as in (3.10); and V_{mid} is the common-mode voltage obtained from (3.21). In Figure 3.8(b), $V^*_{\text{a,max}}$, $V^*_{\text{a,min}}$, and $V^*_{\text{a,mid}}$ respectively represent the corresponding reference voltages of phase A when the common-mode voltages are $V_{\text{com, max}}$, $V_{\text{com, min}}$, and V_{mid}. According to (3.28), the adjustable range of the duty cycle (d_{02}) of the last switching state for the common-mode voltage V_{mid} is depicted in Figure 3.8(c), where $\Delta d_{02,\text{ max}}$ and $\Delta d_{02,\text{ min}}$ are respectively the adjustments of d_{02} in order to achieve the maximum and minimum limits of the common-mode voltage. The adjustment (Δd_{02}) of d_{02} can be any value between $\Delta d_{02,\text{ max}}$ and $\Delta d_{02,\text{ min}}$, and this adjustment can be realized in the nearest-level modulation method by tuning V_{mid} based on (3.28).

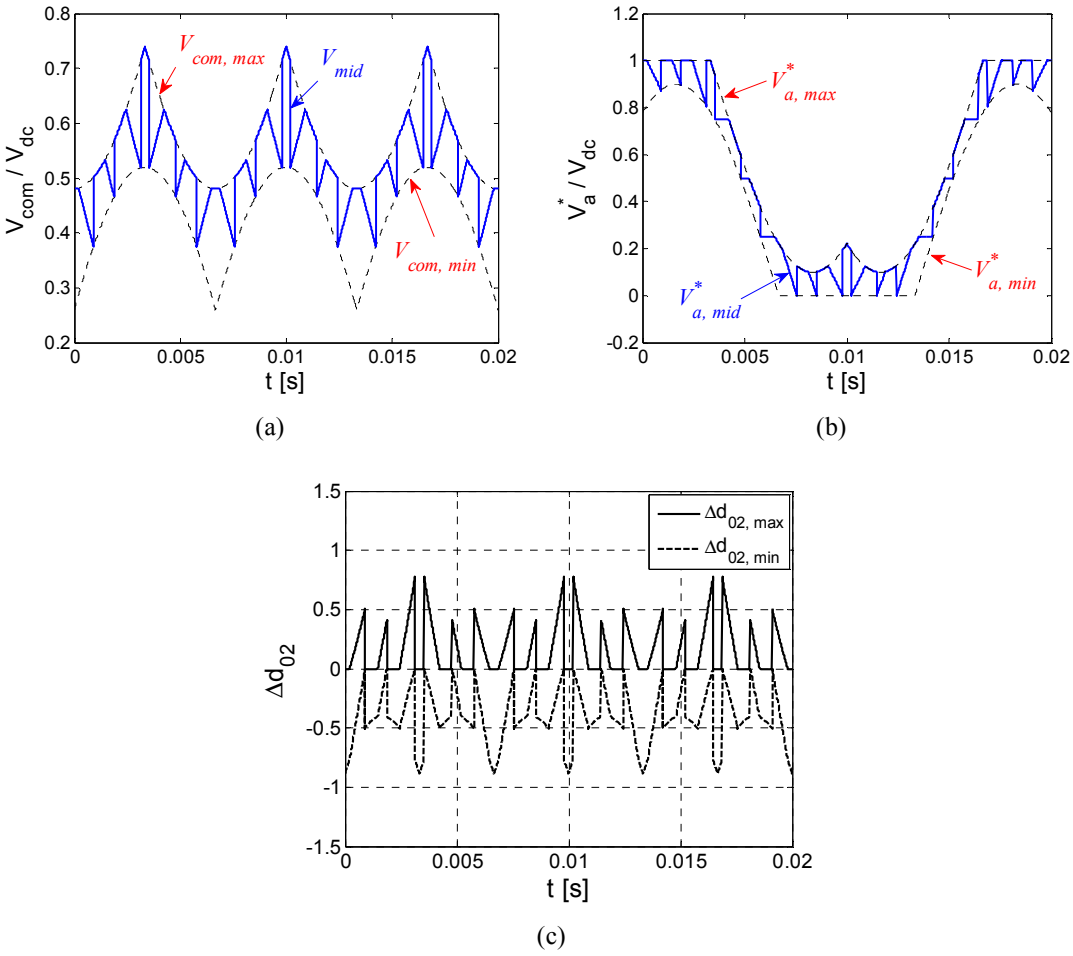


Figure 3.8 An example of the relationship between the common-mode voltage and the duty cycles, for modulation index m=0.9 of a five-level converter: (a) the common-mode voltage V_{mid}; (b) the reference voltage of phase A; (c) the available adjustment region of the duty cycle of the last switching state.

Note that there are generally two types of outermost modulation triangles for any multilevel converter. Figure 3.9 shows the outermost triangles of a five-level converter as an example. For a given reference vector, the type I triangle (with one vertex on the five-level hexagon) leads to two switching sequences for each switching sequence mode, e.g., 031 → 041 → 141 → 142 and 030 → 031 → 041 → 141 for the ascending mode for $\Delta P_1P_2P_3$. The type II triangle (with two vertexes on the five-level hexagon) generates only one switching sequence for each switching sequence mode, e.g., 031 → 041 → 042 → 142 for the ascending mode for $\Delta P_1P_2P_4$. These two types of outermost modulation

triangles are reflected by the relationship between $V_{\text{com, max}}$ and V_{mid} in Figure 3.8. If $V_{\text{mid}} < V_{\text{com, max}}$, then the reference vector is located in a type I triangle, and the maximum and minimum limits of the common-mode voltage cause different switching sequences. In contrast, when $V_{\text{mid}} = V_{\text{com, max}}$, the reference vector is located in a type II triangle. The following common-mode voltages make the duty cycles of the first and the last switching states in each switching sequence to be equal, for a type I triangle:

$$V_{com1} = 0.5\left(V_{mid} + V_{com,min}\right) \tag{3.29a}$$

$$V_{com2} = 0.5\left(V_{mid} + V_{com,max}\right) \tag{3.29b}$$

For a type II triangle, only (3.29a) is applied. Similar conclusions can be obtained when the reference vectors are located in the low-modulation regions.

It should be also noted that sometimes the optimized switching sequence [44] [58] discussed in this section may not be adopted by the SVM method. For example, the switching states of the nearest three vectors are selected in [17] for achieving the best capacitor voltage balancing, without considering minimizing the number of switch transitions. The question then is whether the nearest-level modulation method can equivalently realize the SVM method in these conditions? The answer is yes. No matter what switching states are selected by the SVM method, the required reference voltage of each phase can always be generated based on (3.17) for the nearest-level modulation method. Consequently, the switching sequence can be obtained similarly from (3.16) as a reverse process, except that the reference phase voltage may be approximated by other voltage levels instead of the two nearest levels. Figure 3.10 shows a general arrangement of the switching states for the nearest-level modulation method, in order to obtain the switching sequence shown in Figure 3.3(a).

In summary, by selecting the proper common-mode voltage injection and appropriately arranging the switching states and the corresponding duty cycles for each phase, a nearest-level modulation method can equivalently achieve an SVM method.

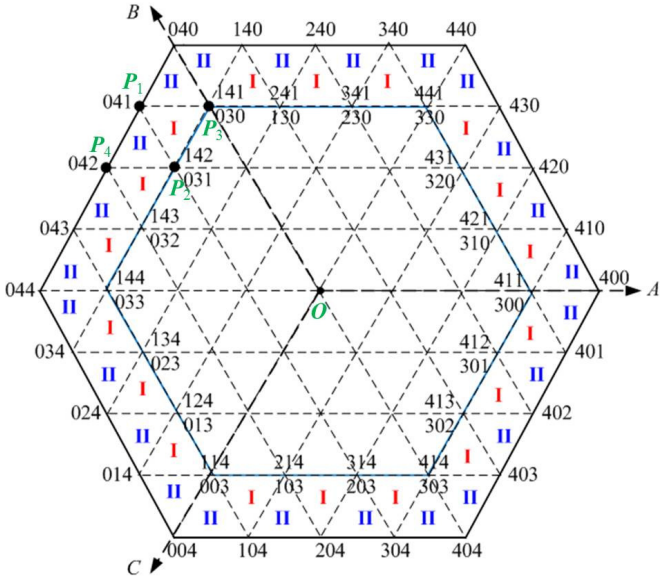


Figure 3.9 Switching states for the outermost modulation triangles of a five-level converter.

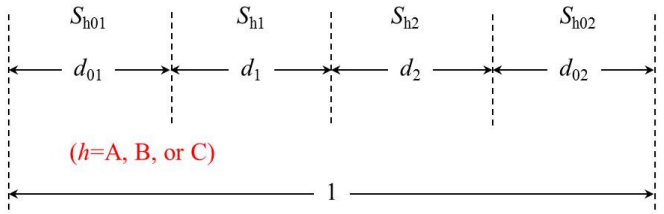


Figure 3.10 Switching states of phase h (h=A, B, or C) for the nearest-level modulation method, in order to obtain the switching sequence generated by the SVM method shown in Figure 3.3(a).

3.4 Respective Advantages of SVM and Nearest-Level Modulation

It has been demonstrated in the previous sections that the SVM and the nearest-level modulation methods can produce identical switching sequences despite their apparent differences. However, due to their respective advantages these two modulation methods have different suitable applications, as introduced below.

3.4.1 Flexible Switching Patterns

Compared to the nearest-level modulation, the SVM method is much more convenient to handle the tasks when particular switching patterns are desired, e.g., in the applications of capacitor voltage balancing for diode-clamped multilevel converters [16]

[17] [83] where the optimal switching sequence and duty cycles are needed. The SVM method can flexibly adjust the redundant switching sequences and duty cycles [44], while the same function achieved by the nearest-level modulation method requires sophisticated selection of the common-mode voltage, as illustrated in Figures 3.5-3.8. Considerable computational effort may be needed by the nearest-level modulation method to search for the best common-mode voltage, especially when the reference vector is located in the low-modulation regions. As explained before, the essential reason is: the common-mode voltage is fixed in the nearest-level modulation method, while it can be any value in the SVM method.

3.4.2 Computational Complexity

The major advantage of the nearest-level modulation method is the less computational burden compared to previous SVM methods. However, the fast and generalized SVM method proposed in [44] has overcome the drawbacks of the previous SVM methods and achieved the same time complexity [i.e., O(n), where n is the level number of the converter] with the nearest-level modulation method, if the nearest-level modulation method is also desired to generate all the redundant switching sequences. Therefore, computational complexity is no longer an obstacle for the SVM method. The SVM method in [44] can be further simplified for three-phase multilevel applications, which will be introduced in future papers.

3.4.3 Multiphase Multilevel Applications

Since the nearest-level modulation method directly controls the voltage of each phase, it is more suitable than the SVM method for multiphase multilevel applications. Based on the relationship between the two modulation methods established in the previous sections, an efficient and flexible modulation method for any multiphase multilevel converter is proposed as follows. It combines the advantages of the nearest-level modulation and the

SVM methods, i.e., both with less computational burden and high flexibility of optimizing the switching patterns.

For a p-phase n-level converter, the reference voltage V_i^* of phases i (i=1, 2, … p) is

$$V_i^* = m \cdot V_{dc} \cos\left(\theta - (i-1) \cdot \frac{2\pi}{p}\right) + V_{com} \tag{3.30}$$

Assume the duty cycles D_i of phase i (i=1, 2, … p) obtained from (3.8) have the following relationship

$$D_1 \leq D_2 \leq \cdots \leq D_p \tag{3.31}$$

which leads to two switching sequences in two modes (descending and ascending modes) similar to (3.16), but now there are p+1 switching states in each switching sequence. As discussed before, for each valid switching sequence, the duty cycles of the middle switching states are constant. Therefore, only the duty cycles (i.e., D_1 and 1-D_p) of the first and the last switching states need to be adjusted, and the summation of these two duty cycles should be kept constant.

If the redundant switching sequences similar to (3.13) are required, or the duty cycles of the first and the last switching states need to be tuned, then the corresponding adjustment of the common-mode voltage is [similar to (3.28)]

$$\Delta V_{com} = (k + \Delta d) \cdot V_{dc}/(n-1) \tag{3.32}$$

where k denotes the change of the redundant switching states as in (3.13); and Δd represents the adjustment for the duty cycle of the switching state [K_1+1, K_2+1, …, K_p+1]^T, i.e., the first switching state if (3.16a) is adopted (descending mode), or the last switching state if (3.16b) is adopted (ascending mode). The feasible range of Δd is

$$-D_1 \leq \Delta d \leq 1 - D_p \tag{3.33}$$

In summary, the proposed multiphase multilevel modulation method contains the following steps:

1) Step 1: Select a typical common-mode voltage. Calculate the switching states and the duty cycles based on (3.7) and (3.8).

2) Step 2: Arrange the switching states and duty cycles of each phase as in (3.16).

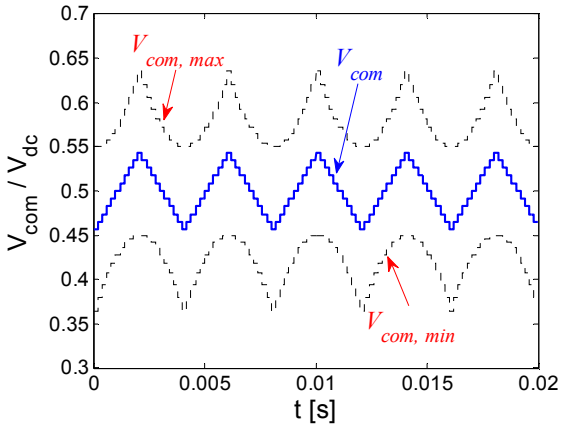
3) Step 3: If needed, adjust the common-mode voltage within its feasible region [similar to (3.10)] according to (3.32).

4) Step 4: Generate the reference voltage for each phase from (3.30) based on the adjusted common-mode voltage.

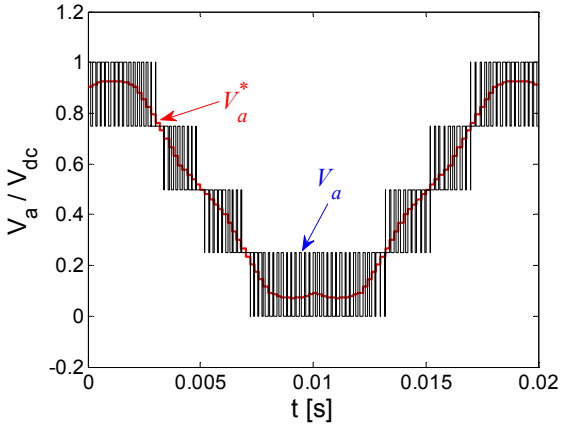
Figure 3.11 demonstrates the simulated output waveforms of a five-phase five-level converter as an example, when the modulation index is m=0.45, for a typical common-mode voltage:

$$V_{com} = 0.5\left(V_{com,max} + V_{com,min}\right) \tag{3.34}$$

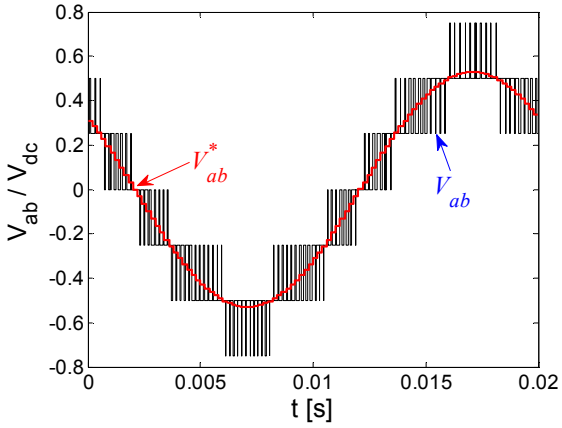
where $V_{\text{com, max}}$ and $V_{\text{com, min}}$ are respectively the maximum and minimum limits of the common-mode voltage. The fundamental frequency and switching frequency in the simulation are 50 Hz and 5 kHz, respectively. In the figures, V_{a}^{*} and V_{a} respectively denote the reference and the actual output voltages of the 1st phase; V_{ab}^{*} $(= V_{\text{a}}^{*} - V_{\text{b}}^{*})$ and V_{ab} respectively represent the reference and the actual output line-to-line voltages (1st phase to 2nd phase).



(a)



(b)



(c)

Figure 3.11 Simulated output waveforms of a 5-phase 5-level converter for the common-mode voltage in (3.34) when modulation index m=0.45: (a) the common-mode voltage; (b) the output voltage of the 1st phase; (c) the line-to-line voltage (1st phase to 2nd phase).

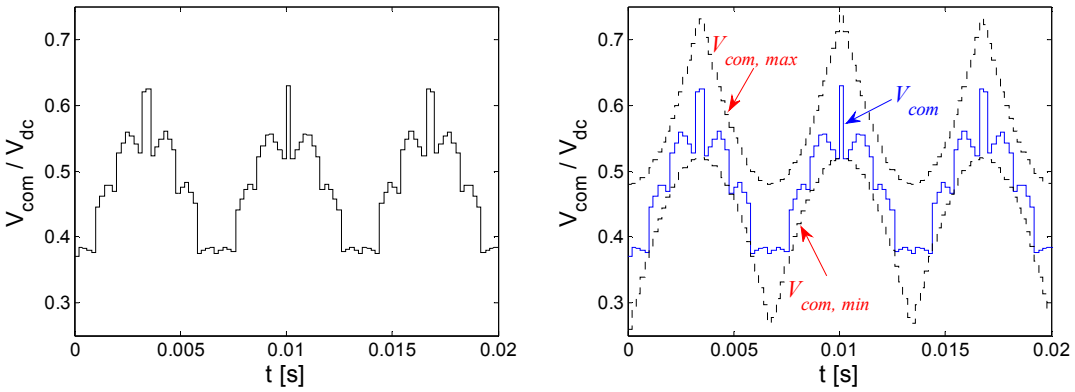
3.5 Simulation and Experimental Results

It has been demonstrated in the previous sections that the SVM and the nearest-level modulation methods can produce identical switching sequences despite their apparent differences. However, due to their respective advantages these two modulation methods have different suitable applications, as introduced below.

3.5.1 Simulation Results

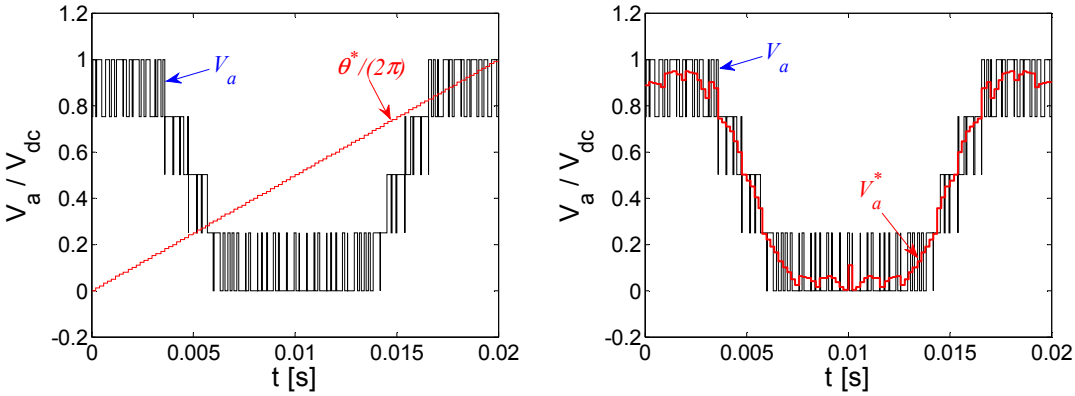
Simulations are implemented in MATLAB/Simulink for a three-phase five-level converter, to compare the SVM [44] and the nearest-level modulation methods. In the simulation, the switching frequency is 5 kHz (fundamental frequency is 50 Hz), the modulation index is 0.9, and the duty cycles of the first and the last switching states in each switching sequence are equal.

Figure 3.12 illustrates the common-mode voltage V_{com} for this operating condition, calculated in two ways: a) based on (3.17) for each switching sequence generated by the SVM method; b) obtained from (3.29) based on the equivalence of the nearest-level modulation method. It is seen that these two ways give exactly the same result of the common-mode voltage. Figure 3.13(a) shows the phase voltage V_a (phase A) of the converter generated by the SVM method, where θ^* is the corresponding reference phase angle in (3.5). Based on the common-mode voltage shown in Figure 3.12(b), the same phase voltage is produced by the nearest-level modulation method as illustrated in Figure 3.13(b), where V_a^* is the reference phase voltage. The simulation results in Figures 3.12 and 3.13 demonstrate the equivalence of the two modulation methods.



(a) (b)

Figure 3.12 The common-mode voltage obtained from different ways: (a) the SVM method in [44]; (b) the relationship in (3.29).



(a) (b)

Figure 3.13 Simulated phase A voltage of the five-level converter in MATLAB Simulink: (a) the SVM method in [44]; (b) the nearest-level modulation method.

3.5.2 Experimental Results

An experiment is also carried out based on a TMS320CF2812 DSP (digital signal processor) to demonstrate the equivalence between the SVM method [44] and the nearest-level modulation method. The experiment is implemented by first running the SVM and then the nearest-level modulation algorithm on the DSP in real time for any received reference voltage, for the three-phase five-level converter. The DSP does not send gate signals to drive any power electronic switches, but instead sends the switching

states generated by the two modulation algorithms to a digital-to-analog converter for observation, which represent the voltages of the converter as described in (3.1). An actual converter is not required for this experiment.

For the experiment, the switching frequency is 500 Hz in order to highlight the switch transitions. Other operation conditions are the same as that adopted in the simulations; again, the common-mode voltage obtained from (3.29) is applied to the nearest-level modulation method. Figure 3.14 demonstrates the corresponding experimental results from the DSP outputs of the SVM method and the nearest-level modulation method, which also indicate the equivalence of the two modulation methods.

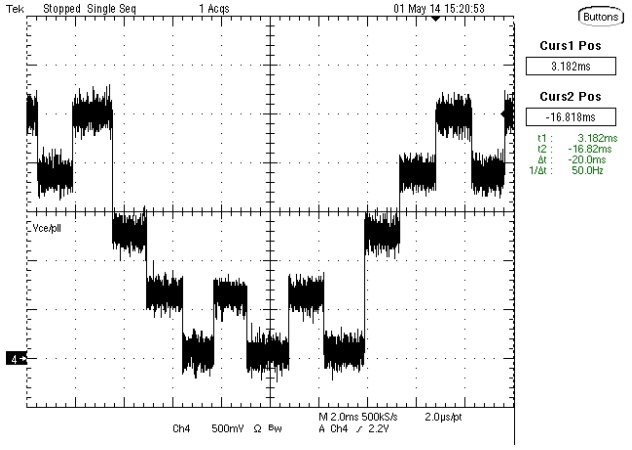


Figure 3.14 Experimental results from the DSP outputs of the phase voltage (phase A) for the five-level converter, represented by the corresponding switching states generated by the two modulation methods: (a) the SVM method in [44]; (b) the nearest-level modulation method.

3.6 Chapter Summary

This chapter has studied the inherent relationship between the space vector modulation (SVM) method and the nearest-level modulation method for multilevel converters. It is concluded that the SVM and the nearest-level modulation methods are functionally equivalent: 1) by injecting the proper common-mode voltage, the nearest-level modulation method can equivalently realize the SVM method; 2) by selecting the appropriate redundant switching sequence and duty cycles (of the first and the last switching states in each switching sequence), the SVM method can equivalently realize the nearest-level modulation method. Simulation and experimental results validate the analysis.

However, these two modulation methods have different suitable applications, due to their respective advantages. The SVM method is much more convenient to handle the tasks when particular switching patterns are desired, e.g., in the application of capacitor voltage balancing for multilevel converters where the optimal switching sequence and duty cycles are preferred. The essential reason is: the common-mode voltage is fixed in the nearest-level modulation method, while it can be any value in the SVM method. In contrast, because of the phase-voltage modulation approach, it is more suitable for the nearest-level modulation method to apply to multiphase multilevel converters.

Based on the relationship between the nearest-level modulation and the SVM described in this chapter, a general and flexible modulation method for any multiphase multilevel converter has been proposed. It combines the advantages of the nearest-level modulation and the SVM methods, i.e., both with less computational burden and high flexibility of optimizing the switching patterns. The adjustment rule of the common-mode voltage, for achieving the desired redundant switching sequences and tuning the corresponding duty cycles, has been established.

The next chapter proposes a simplified SVM scheme for multilevel converters, based on the findings in this chapter.

CHAPTER 4 A SIMPLIFIED SPACE VECTOR MODULATION SCHEME FOR MULTILEVEL CONVERTERS

This chapter proposes a simplified space vector modulation (SVM) scheme for multilevel converters, based on the findings in Chapter 3. Compared with earlier SVM methods, the proposed scheme in this chapter simplifies the detection of the nearest three vectors and the generation of switching sequences, and therefore is computationally more efficient. Particularly, for the first time, the proposed scheme achieves the same easy implementation as phase-voltage modulation techniques. Another superior characteristic of the proposed scheme over earlier methods is its potential for multiphase multilevel applications. The proposed scheme also offers the following significant advantages: 1) independence of the level number of the converter; 2) more degrees of freedom, i.e., redundant switching sequences and adjustable duty cycles, to optimize the switching patterns; and 3) no need for lookup tables or coordinate transformations. These advantages make the proposed scheme well suited to large level-number applications, such as modular multilevel converters (MMCs) and high voltage direct current (HVDC) systems. Simulation and experimental results verify this new concept.

Figure 4.1 shows the functional diagram of an SVM-based three-phase n-level converter, where the single-pole n-throw switch represents the functionality of each converter phase. There generally are n^3 switching states and $6(n\text{-}1)^2$ triangles in the space vector diagram of a three-phase n-level converter [44]; a reference vector can be located within any triangle. To achieve the same volt-second average as the reference vector, it is the task of SVM to select suitable switching states of the located triangle (its vertices are the "nearest three vectors") and execute them for respective needed durations (duty cycles) in an appropriate sequence (switching sequence).

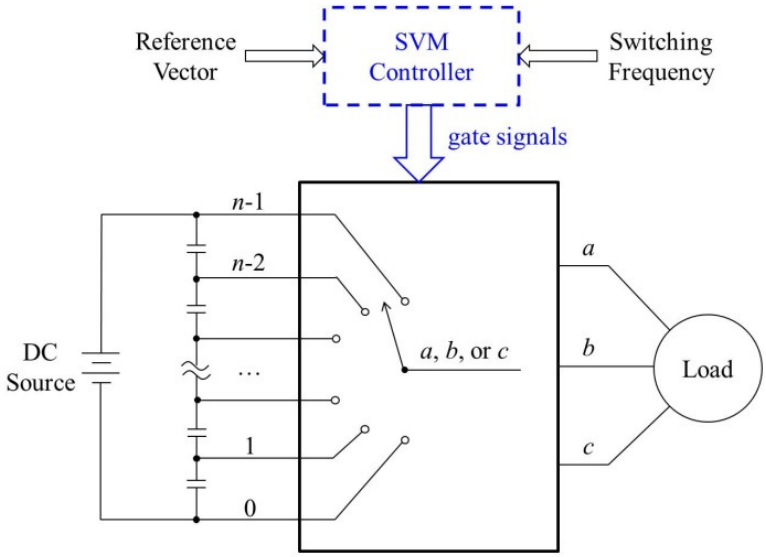


Figure 4.1 Functional diagram of a three-phase *n*-level converter.

4.1 Orthogonal Unit-Vectors

This section introduces a general approach to construct orthogonal unit-vectors for different multiphase systems, as illustrated in Figure 4.2. The objective is to decouple the components of different phases, so as to implement the SVM based on the commonly-used α-β coordinates.

4.1.1 Three-Phase System

For the three-phase *n*-level converter shown in Figure 4.1, a reference vector is generated [38] [44] as

$$\boldsymbol{V}_{ref} = (n-1)\left(V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi}\right) = (n-1)\left(m \cdot \frac{\sqrt{3}}{2} V_{dc} \cdot e^{j\theta}\right) \tag{4.1}$$

where V_{a}^*, V_{b}^*, and V_{c}^* are respectively the reference voltages of phases *a*, *b*, and *c* relative to the negative terminal of the dc-link; V_{dc} is the dc-link voltage of the converter; m is the modulation index; and θ is the phase angle of the phase *a* voltage. According to (4.1), any reference vector is constructed by three "unit-vectors" $\boldsymbol{V}_{\mathrm{a}}$, $\boldsymbol{V}_{\mathrm{b}}$, and $\boldsymbol{V}_{\mathrm{c}}$ of the three phases, where

$$\begin{bmatrix} \boldsymbol{V}_a \\ \boldsymbol{V}_b \\ \boldsymbol{V}_c \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 \\ e^{j\frac{2}{3}\pi} \\ e^{j\frac{4}{3}\pi} \end{bmatrix} \tag{4.2}$$

The coupling of the three-phase components, when composing the reference vector, leads to the difficulty in detecting the positions of the nearest three vectors. If the reference vector can be decomposed into orthogonal coordinates, where the component of each phase is only contained in one of the coordinates (i.e., the three phases are "decoupled"), then the component related to each phase can be directly obtained from the decomposition. As shown in Figure 4.2(a), two such orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ corresponding to the real and imaginary axes (i.e., the α-β frame) are defined as

$$\begin{bmatrix} \boldsymbol{V}_x \\ \boldsymbol{V}_y \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a \\ \boldsymbol{V}_b - \boldsymbol{V}_c \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 \\ j\sqrt{3} \end{bmatrix} \tag{4.3}$$

The basic concept of constructing these orthogonal unit-vectors can be summarized as follows: 1) a unit-vector in the direction of the real or imaginary axis is already an orthogonal component; 2) if a unit-vector is not laid on the real or imaginary axis, then it can be combined with another unit-vector (these two unit-vectors are symmetrical with respect to the real or imaginary axis) to compose an orthogonal component.

According to the two orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$, the real and imaginary coordinates (i.e., x and y, respectively) of the reference vector $\boldsymbol{V}_{ref}$ are

$$x = \frac{V_{ref(x)}}{V_{dc}}, \quad y = \frac{V_{ref(y)}}{\sqrt{3}V_{dc}} \tag{4.4}$$

where $V_{ref(x)}$ and $V_{ref(y)}$ are respectively the real and imaginary components of the reference vector. When $\boldsymbol{V}_{ref}$ is located in over-modulation regions, it can be modified similarly as in [44].

Afterwards, based on the definition of $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ in (4.3), a new set of reference voltages for the three phases can be easily obtained as follows (though not actually needed in the proposed scheme) from the reference vector as a reverse process:

$$\begin{bmatrix} V_{a0}^* \\ V_{b0}^* \\ V_{c0}^* \end{bmatrix} = \frac{1}{n-1}\begin{bmatrix} x \cdot V_{dc} \\ y \cdot V_{dc} \\ -y \cdot V_{dc} \end{bmatrix} = \frac{1}{n-1}\begin{bmatrix} V_{ref(x)} \\ V_{ref(y)}/\sqrt{3} \\ -V_{ref(y)}/\sqrt{3} \end{bmatrix} \tag{4.5}$$

For an SVM scheme, this new set of reference voltages $\{V_{a0}^*, V_{b0}^*, V_{c0}^*\}$ is equivalent to the original reference voltage set $\{V_a^*, V_b^*, V_c^*\}$ in (4.1), as they generate the same reference vector.

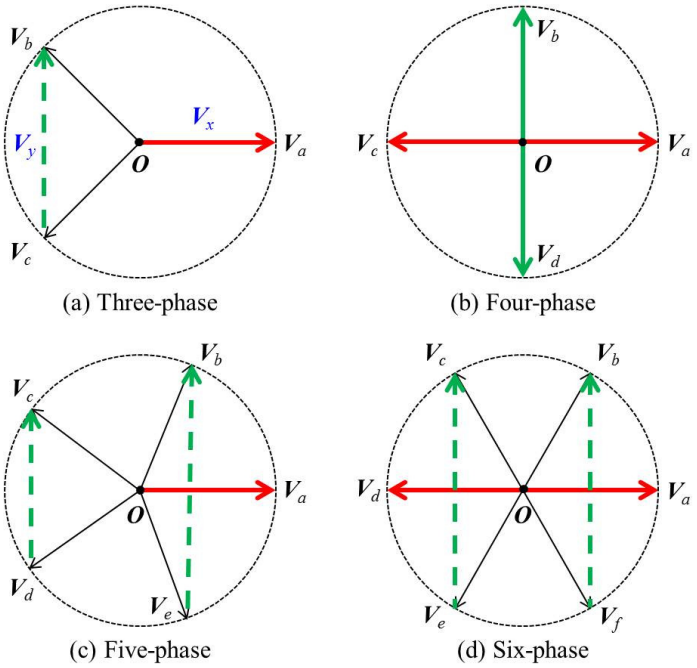


Figure 4.2 Orthogonal unit-vectors for different multiphase systems.

4.1.2 Multiphase System

The aforementioned concept of constructing the orthogonal unit-vectors can be easily extended to other multiphase systems. For example, Figure 4.2 also demonstrates the orthogonal unit-vectors for four-, five-, and six-phase systems, where the bolded arrows represent the orthogonal components (the dashed arrows are composed by two unit-vectors).

The orthogonal unit-vectors for four-, five-, and six-phase systems are respectively as follows

$$\begin{bmatrix} \boldsymbol{V}_{x4} \\ \boldsymbol{V}_{y4} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a - \boldsymbol{V}_c \\ \boldsymbol{V}_b - \boldsymbol{V}_d \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 2 \\ j2 \end{bmatrix} \tag{4.6a}$$

$$\begin{bmatrix} \boldsymbol{V}_{x5} \\ \boldsymbol{V}_{y5} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a \\ \boldsymbol{V}_b - \boldsymbol{V}_e + \boldsymbol{V}_c - \boldsymbol{V}_d \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 \\ j2(\sin(0.2\pi) + \sin(0.4\pi)) \end{bmatrix} \tag{4.6b}$$

$$\begin{bmatrix} \boldsymbol{V}_{x6} \\ \boldsymbol{V}_{y6} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a - \boldsymbol{V}_d \\ \boldsymbol{V}_b - \boldsymbol{V}_f + \boldsymbol{V}_c - \boldsymbol{V}_e \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 2 \\ j2\sqrt{3} \end{bmatrix} \tag{4.6c}$$

Note that the orthogonal unit-vectors may be constructed in different ways. For example, Figure 4.3 shows another candidate choice of the orthogonal unit-vectors for the five-phase system:

$$\begin{bmatrix} \boldsymbol{V}'_{x5} \\ \boldsymbol{V}'_{y5} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a - \boldsymbol{V}_c - \boldsymbol{V}_d \\ \boldsymbol{V}_b - \boldsymbol{V}_e \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 + 2\cos(0.2\pi) \\ j2\sin(0.4\pi) \end{bmatrix} \tag{4.7}$$

Similar to the discussion in (4.5), the equivalent reference voltages for all the phases can always be recovered as a reverse process, no matter what set of orthogonal unit-vectors is adopted. Therefore, the different constructions of orthogonal unit-vectors have no influence on the accuracy.

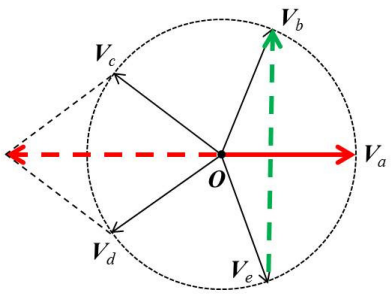


Figure 4.3 Another two orthogonal unit-vectors for the five-phase system.

4.2 Proposed SVM Scheme

Figure 4.4 shows the proposed *n*-level SVM scheme, based on the space vector diagram of a five-level converter. Increasing the level number by one always forms an additional hexagonal ring of equilateral triangles, which surrounds the outermost hexagon H_0. Figure 4.4 is explained later in detail. The proposed scheme works for all the

multilevel converter topologies (i.e., diode/capacitor-clamped, cascaded H-bridge, and MMC), since they have the same space vector diagram.

Corresponding to (4.1), an output space vector that represents the switching states of all the phases is defined for a three-phase n-level converter [38] [44] as

$$\boldsymbol{V}_{out} = V_{dc} \cdot \left(S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi} \right) \tag{4.8}$$

where S_a, S_b, and S_c (S_a, S_b, S_c=0, 1, …n-1) are the switching states of phases a, b, and c, respectively. Accordingly, the voltage of phase h (h=a, b, or c) relative to the negative terminal of the dc-link is $S_h \cdot V_{dc}/(n\text{-}1)$. The definition in (4.8) causes the side length of each modulation triangle (e.g., $\Delta P_1P_2P_3$) in the space vector diagram to be V_{dc}.

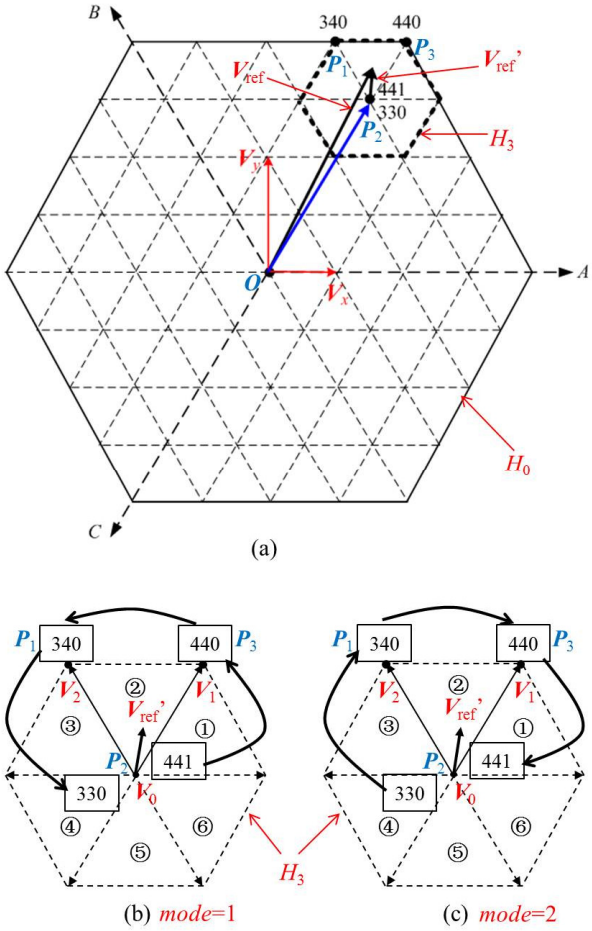


Figure 4.4 The proposed SVM scheme: (a) detecting the modulation triangle; (b)-(c) two switching sequence modes.

All the output space vectors of the converter compose the space vector diagram, where the number at each vertex (e.g., 340 at P_1) represents the switching state $S_aS_bS_c$ of the corresponding space vector. Some space vectors can be equivalently produced by more than one switching state; those switching states are called redundant switching states, and are listed decreasingly from top to bottom corresponding to the switching states of phase *a*. For example, 441 and 330 are both valid switching states of the space vector $\boldsymbol{OP}_2$.

In order to synthesize the reference vector $\boldsymbol{V}_{\text{ref}}$ defined in (4.1), it is the task of the SVM scheme to detect the modulation triangle $\Delta P_1P_2P_3$ (i.e., the nearest three vectors $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$), to calculate the duty cycles (needed durations) of the nearest three vectors, and to determine the switching sequence (switching state sequence of the nearest three vectors). The synthesis is based on achieving the same volt-second average [38] [44]

$$\boldsymbol{V}_{ref} = D_1 \cdot \boldsymbol{OP}_1 + D_2 \cdot \boldsymbol{OP}_2 + D_3 \cdot \boldsymbol{OP}_3 \tag{4.9}$$

where D_1, D_2, and D_3 are the duty cycles of $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$, respectively. Normally, to ensure the minimum number of switch transitions in every switching cycle, the optimized switching sequences [38] [44] [58] are required.

4.2.1 Detecting the Nearest Three Vectors

It should be noted that unlike earlier SVM methods, only one of the nearest three vectors (e.g., $\boldsymbol{OP}_2$) needs to be detected in the proposed scheme. A simple mapping subsequently generates the switching sequences, based on the detected nearest vector. An alternative way to directly detect all the nearest three vectors is introduced in Appendix A.

The two orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ defined in (4.3) are illustrated in Figure 4.4(a). According to these two orthogonal unit-vectors, the real and imaginary coordinates of the reference vector $\boldsymbol{V}_{\text{ref}}$ (i.e., *x* and *y*, respectively) are obtained from (4.4). Afterwards, the vertex (i.e., P_2 as in Figure 4.4) of the modulation triangle $\Delta P_1P_2P_3$, that is closest to the origin *O* of the space vector diagram, can be easily detected as follows.

At first, it is observed from (4.3) that the three-dimensional coordinates (i.e., corresponding to the three unit-vectors $\boldsymbol{V}_a$, $\boldsymbol{V}_b$, and $\boldsymbol{V}_c$ in the original *ABC*-frame) of the two orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ are $[1,\ 0,\ 0]^T$ and $[0,\ 1,\ -1]^T$, respectively. Therefore, a three-dimensional coordinate of the reference vector $\boldsymbol{V}_{ref}$ is $[x,\ y,\ -y]^T$, as discussed in (4.5). Since $\boldsymbol{V}_a + \boldsymbol{V}_b + \boldsymbol{V}_c = \boldsymbol{0}$, equally adjusting the three components of $[x,\ y,\ -y]^T$ generates another three-dimensional coordinate of $\boldsymbol{V}_{ref}$. The objective is to select an appropriate adjustment, so as to easily detect the switching states of a nearest vector.

Consequently, a candidate switching state $S_aS_bS_c$ for the vertex (i.e., P_2) of the modulation triangle $\Delta P_1P_2P_3$ closest to the origin is directly obtained as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \min(x, y, -y) \\ y - \min(x, y, -y) \\ -y - \min(x, y, -y) \end{bmatrix}\right) \tag{4.10}$$

where $\min(x,\ y,\ -y)$ denotes the minimum value among x, y, and $-y$; $\text{int}(\gamma)$ stands for the corresponding integer parts of all the elements in an array γ. As shown in Figure 4.5, any space vector is located on a hexagon (H_0, H_{m1}, H_{m2}, and H_S) that centers at the origin. "Closest to the origin" means that the hexagon on which the detected vertex is located is the smallest among that of the nearest three vectors (e.g., the hexagon H_{m1} is smaller than H_0). Note that the computational burden of (4.10) is independent of the level number of the converter or the location of the reference vector.

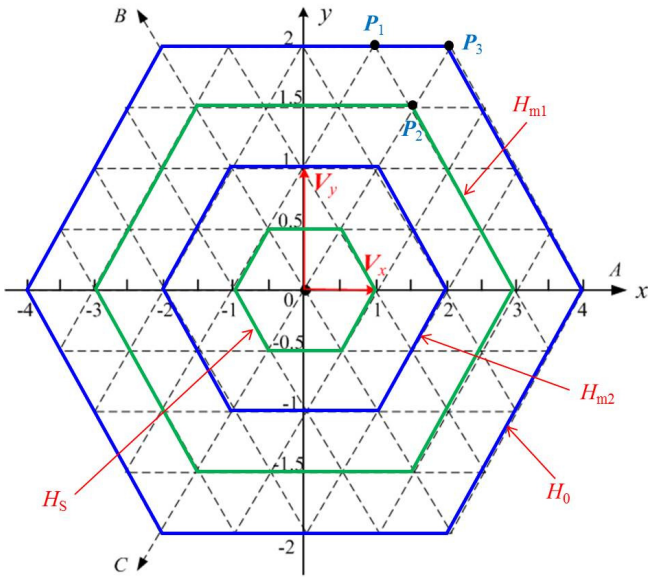


Figure 4.5 Coordinates of the space vectors according to the orthogonal unit-vectors V_x and V_y.

The rationale for (4.10) can be explained as follows. Wherever the reference vector is located, the candidate switching state $S_aS_bS_c$ only has the following values:

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} 0 \\ y - \text{x} \\ -y - \text{x} \end{bmatrix}\right), \quad \text{if } \min(x, y, -y) = x \tag{4.11a}$$

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \text{y} \\ 0 \\ -2y \end{bmatrix}\right), \quad \text{if } \min(x, y, -y) = y \tag{4.11b}$$

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} x + y \\ 2y \\ 0 \end{bmatrix}\right), \quad \text{if } \min(x, y, -y) = -y \tag{4.11c}$$

Figure 4.5 shows the coordinates of the space vectors according to $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$. An important fact is seen from Figure 4.5 that x-min(x, y, -y), y-min(x, y, -y), and -y-min(x, y, -y) are all integers for the three vertices of any modulation triangle. In the coordinate system with the basis set $\{\boldsymbol{V}_x, \boldsymbol{V}_y\}$, there are two types of modulation triangles (i.e., the upward "I" and the downward "II" triangles as in Figure 4.6) in the space vector diagram. Figure 4.6 shows that for an area enclosed by either type of modulation triangle, x-min(x, y, -y), y-min(x, y, -y), and -y-min(x, y, -y) produce their maximum and minimum values at

the three vertices of the triangle; the difference between the maximum and the corresponding minimum value is always one. Therefore, the candidate switching state obtained from (4.10) gives the result of one nearest vector, regardless of the location of the reference vector.

Due to the adoption of min(x, y, $-y$), this detected vector is the vertex of the modulation triangle that is closest to the origin. Figure 4.7 illustrates the nearest vector detected by (4.10) for different locations of the reference vector according to (4.11), where Q_1 and Q_2 are the vertices detected for the areas enclosed by the upward and downward triangles, respectively. The dashed lines represent the minimum values of x-min(x, y, $-y$), y-min(x, y, $-y$), and $-y$-min(x, y, $-y$) for the areas enclosed by each type of triangle. For example, when the angle of the reference vector is $120^\circ \le \theta \le 240^\circ$, (4.11a) applies; the vertex Q_1 (or Q_2), where y-x and $-y$-x both reach their minimum, is detected for the upward (or downward) triangle.

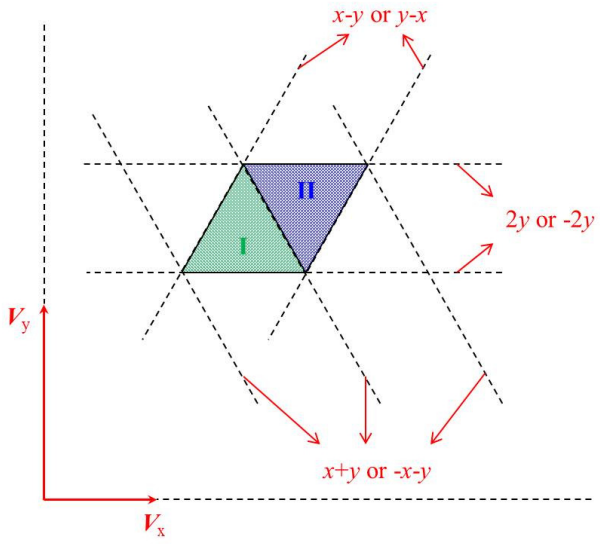


Figure 4.6 Limits of x-min(x, y, $-y$), y-min(x, y, $-y$), and $-y$-min(x, y, $-y$).

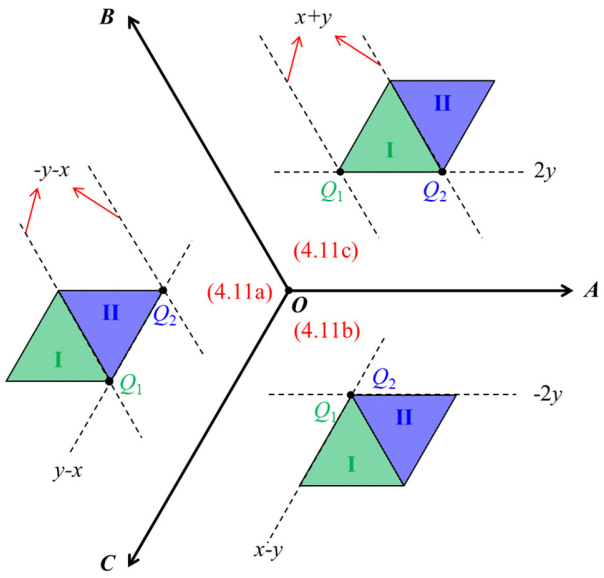


Figure 4.7 The vertex detected by (4.10) for different locations of the reference vector.

Finally, all the available switching states for the vertex (P_2) of the modulation triangle $\Delta P_1P_2P_3$ closest to the origin can be generated as

$$[N + S_a,\ N + S_b,\ N + S_c]^T, \quad \text{where the integer } N \in [0,\ n - 1 - \max(S_a, S_b, S_c)] \tag{4.12}$$

where max(S_a, S_b, S_c) is the maximum value among S_a, S_b, and S_c. Since the vertex closer to the origin has more valid switching states (e.g., P_2 has more valid switching states than P_1 and P_3), detecting this vertex leads to the maximum number of switching sequences.

Consider, for example, the reference vector $\boldsymbol{V}_{ref}$ in Figure 4.4, which has the value of

$$\boldsymbol{V}_{ref} = V_{dc} \cdot (1.55 + 1.75 \cdot j\sqrt{3}) \tag{4.13}$$

From (4.4), the real and imaginary coordinates of the reference vector are x=1.55 and y=1.75. Therefore a candidate switching state $S_aS_bS_c$ for P_2 is obtained from (4.10) as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} 1.55 - \min(1.55, 1.75, -1.75) \\ 1.75 - \min(1.55, 1.75, -1.75) \\ -1.75 - \min(1.55, 1.75, -1.75) \end{bmatrix} \right) = \begin{bmatrix} 3 \\ 3 \\ 0 \end{bmatrix} \tag{4.14}$$

In fact, for any reference vector located inside the triangle $\Delta P_1P_2P_3$, min(x, y, -y) = -y since x>0 and y>0, and

$$3 < x + y < 4, \quad 3 < 2y < 4 \tag{4.15}$$

So wherever the reference vector is located, a candidate switching state 330 will always be generated according to (4.11c), which means that the vertex (i.e., P_2) of the modulation triangle closest to the origin will always be captured. Eventually, all the available switching states for P_2 are generated by (4.12), as 441 and 330 shown in Figure 4.4. The result can be verified by comparison with the space vector diagram of five-level converters [44].

4.2.2 Calculating the Duty Cycles

Once a vertex (closest to the origin O) of the modulation triangle is detected, the origin of the reference vector $\boldsymbol{V}_{\text{ref}}$ is shifted to the detected vertex (i.e., P_2 as in Figure 4.4), which yields a "remainder vector" $\boldsymbol{V}_{\text{ref}}'$ as

$$\boldsymbol{V}_{ref}{}' = \boldsymbol{V}_{ref} - \boldsymbol{OP}_2 \tag{4.16}$$

where $\boldsymbol{OP}_2$ is obtained by substituting the switching state $S_aS_bS_c$ produced by (4.10) into (4.8). Since $\boldsymbol{V}_{\text{ref}}'$ is inside a two-level hexagon (i.e., H_3 as in Figure 4.4) that centers at the detected vertex, the duty cycles of the nearest three vectors are determined in the same way as for a two-level SVM, regardless of the level number of the converter.

As shown in Figure 4.4, $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, and $\boldsymbol{V}_2$ respectively represent the nearest three vectors $\boldsymbol{OP}_2$, $\boldsymbol{OP}_3$, and $\boldsymbol{OP}_1$ as follows:

$$\boldsymbol{V}_0 = \boldsymbol{OP}_2 - \boldsymbol{OP}_2 = \boldsymbol{0}, \quad \boldsymbol{V}_1 = \boldsymbol{OP}_3 - \boldsymbol{OP}_2, \quad \boldsymbol{V}_2 = \boldsymbol{OP}_1 - \boldsymbol{OP}_2 \tag{4.17}$$

The region number *reg* (①-⑥) of the remainder vector $\boldsymbol{V}_{\text{ref}}'$ in the two-level hexagon H_3 is given [44] by

$$reg = \text{int}(3\theta_{rem}/\pi) + 1 \tag{4.18}$$

where θ_{rem} ($0 \le \theta_{\text{rem}} < 2\pi$) is the angle of the remainder vector with respect to the real axis, and $\text{int}(3\theta_{\text{rem}}/\pi)$ represents the integer part of $3\theta_{\text{rem}}/\pi$. An alternative way to calculate *reg* is introduced in Appendix A, which avoids the inverse trigonometric computation.

The corresponding duty cycles are then conveniently obtained [44] as

$$\begin{cases} d_1 = \frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg}{3}\pi\right) - V_{ry}\cos\left(\frac{reg}{3}\pi\right)\right] \\ d_2 = -\frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg-1}{3}\pi\right) - V_{ry}\cos\left(\frac{reg-1}{3}\pi\right)\right] \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{4.19}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{ref}'/V_{dc}$, respectively; d_1 and d_2 are respectively the duty cycles of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$; d_0 is the total duty cycle for the "zero vectors", i.e., the switching states at the detected vertex (e.g., 441 and 330 at P_2). This proposed SVM scheme applies two zero vectors (i.e., two redundant switching states) in each switching sequence. The duty cycles d_{01} and d_{02} of the two zero vectors can be freely adjusted [44] as long as

$$d_{02} = d_0 - d_{01}, \quad 0 \le d_{01} \le d_0 \tag{4.20}$$

Note that no real-time trigonometric calculation is needed for (4.19), since *reg* only has six integer values (i.e., from one to six). The six possible values of $\sin(\pi \cdot reg/3)$ and $\cos(\pi \cdot reg/3)$ can be pre-calculated.

4.2.3 Generating the Switching Sequences

Based on the switching states of the detected nearest vector (e.g., $\boldsymbol{OP}_2$) and the region number *reg* of the remainder vector $\boldsymbol{V}_{ref}'$, all the switching sequences can now be generated. There are two switching sequence modes for selection, i.e., *mode*=1 when the switching sequence is counterclockwise ($d_{01}*\boldsymbol{V}_0 \rightarrow d_1*\boldsymbol{V}_1 \rightarrow d_2*\boldsymbol{V}_2 \rightarrow d_{02}*\boldsymbol{V}_0$) as in Figure 4.4(b), and *mode*=2 when the switching sequence is clockwise ($d_{02}*\boldsymbol{V}_0 \rightarrow d_2*\boldsymbol{V}_2 \rightarrow d_1*\boldsymbol{V}_1 \rightarrow d_{01}*\boldsymbol{V}_0$) as in Figure 4.4(c).

Table 4.1 gives a general rule of determining the switching sequences, called the "second mapping" in [44]. The basic principle is that the shifting of vectors can be represented by adjusting the switching states of the corresponding phase. Each element of the mapping includes five sub-elements. The letter A, B, or C means that the switching state of phase *a*, *b*, or *c* is to be modified sequentially in order to switch to another nearest vector. The symbol "↑" or "↓" indicates that the switching state of the corresponding

phase is increased or decreased by 1, respectively. For example, if the first switching state (obtained from the detected vertex) of a switching sequence is $S_{a0}S_{b0}S_{c0}$ and the rule is "BAC↑(L)" (i.e., *reg*=2 and *mode*=2), then the switching sequence is generated as $S_{a0}S_{b0}S_{c0} \rightarrow S_{a0}(S_{b0}+1)S_{c0} \rightarrow (S_{a0}+1)(S_{b0}+1)S_{c0} \rightarrow (S_{a0}+1)(S_{b0}+1)(S_{c0}+1)$. As aforementioned, the redundant switching states at each vertex are listed decreasingly from top to bottom corresponding to the switching states of phase *a*. The letter "L" in the parentheses represents the word "lower" and means that the first switching state $S_{a0}S_{b0}S_{c0}$ should not be the top one at the detected vertex, e.g., not 441 for vertex P_2; the letter "U" in the parentheses represents the word "upper" and means that the first switching state $S_{a0}S_{b0}S_{c0}$ should not be the bottom one at the detected vertex, e.g., not 330 for vertex P_2. Accordingly, the switching sequences for the reference vector $\boldsymbol{V}_{ref}$ in Figure 4.4 are generated as 441 → 440 → 340 → 330 (*mode*=1) and 330 → 340 → 440 → 441 (*mode*=2), as shown in Figure 4.4(b) and (c).

Table 4.1 Original Rule of Determining Switching Sequences [44]

	reg					
	1	2	3	4	5	6
mode=1	ABC↑(L)	CAB↓(U)	BCA↑(L)	ABC↓(U)	CAB↑(L)	BCA↓(U)
mode=2	CBA↓(U)	BAC↑(L)	ACB↓(U)	CBA↑(L)	BAC↓(U)	ACB↑(L)

Though the mapping in Table 4.1 generates all the optimized switching sequences [38] [44] [58] (with the minimum number of switch transitions in every switching cycle) for any multilevel converter and reference vector, its implementation is still relatively more complicated than the phase-voltage modulation techniques (carrier-based modulation and nearest-level modulation), because of the encoding (which causes complexity and extra memory consumption in real-time implementation) needed for the four switching states and the respective duty cycles in each switching sequence. An earlier work has demonstrated that SVM and nearest-level modulation produce identical switching

sequences, despite their apparent differences [38]. However, is it possible to simplify the generation of switching sequences for SVM based on the concept of nearest-level modulation? A further simplified mapping summarized in Table 4.2 answers this question, as explained later.

At first, it is observed from Table 4.1 that for the switching state of phase h (h=a, b, or c), there are only two successive values K_h and K_h+1 in each optimized switching sequence [38] [44]; $K_aK_bK_c$ and $(K_a+1)(K_b+1)(K_c+1)$ are the two "zero vectors". Figure 4.8 shows the switching state of each phase according to the "↑" and "↓" switching sequence modes (called the ascending mode and descending mode, respectively) in Table 4.1. As demonstrated in [38], if the respective duty cycles of K_h and K_h+1 (i.e., 1-D_h and D_h) are equal to that of the switching sequence produced by Table 4.1, then the same switching sequence is equivalently achieved in Figure 4.8. For example, when *reg*=2 and *mode*=2, the four switching states and the corresponding duty cycles in the switching sequence are $d_{02}{*}S_{a0}S_{b0}S_{c0} \rightarrow d_2{*}S_{a0}(S_{b0}+1)S_{c0} \rightarrow d_1{*}(S_{a0}+1)(S_{b0}+1)S_{c0} \rightarrow d_{01}{*}(S_{a0}+1)(S_{b0}+1)(S_{c0}+1)$ according to Table 4.1. The same sequence is therefore equivalently achieved in Figure 4.8(a) if K_h=S_{h0} and D_h is the value shown in Table 4.2 (*reg*=2), as demonstrated in Figure 4.9. Finally, Table 4.2 lists the results for all the other cases. The discontinuous SVM patterns [58] (i.e., eliminating either the first or last switching state in each sequence) can be easily achieved by setting d_{01}=0 or d_{01}=d_0.

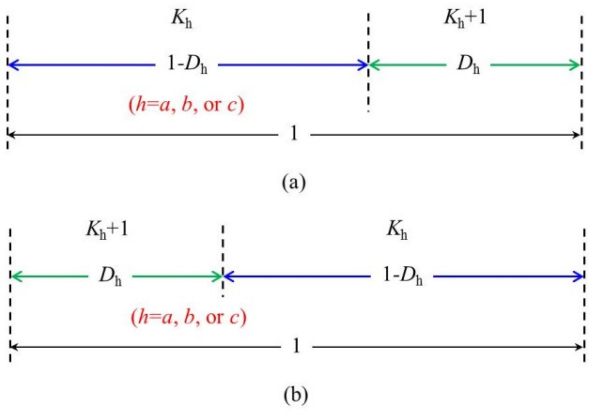


Figure 4.8 The two switching sequence modes: (a) ascending mode (↑); (b) descending mode (↓).

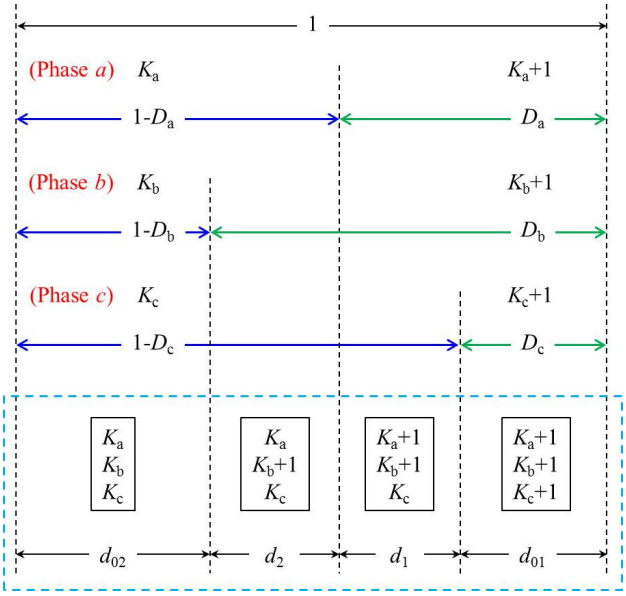


Figure 4.9 Equivalence between the two mappings shown in Tables 4.1 and 4.2, taking *reg*=2 and *mode*=2 as an example.

Table 4.2 Simplified Mapping of Determining Switching Sequences①②

reg	1	2	3	4	5	6
D_h	$D_a = 1\text{-}d_{01}$ $D_b = 1\text{-}d_{01}\text{-}d_1$ $D_c = 1\text{-}d_{01}\text{-}d_1\text{-}d_2$	$D_a = d_{01}+d_1$ $D_b = d_{01}+d_1+d_2$ $D_c = d_{01}$	$D_a = 1\text{-}d_{01}\text{-}d_1\text{-}d_2$ $D_b = 1\text{-}d_{01}$ $D_c = 1\text{-}d_{01}\text{-}d_1$	$D_a = d_{01}$ $D_b = d_{01}+d_1$ $D_c = d_{01}+d_1+d_2$	$D_a = 1\text{-}d_{01}\text{-}d_1$ $D_b = 1\text{-}d_{01}\text{-}d_1\text{-}d_2$ $D_c = 1\text{-}d_{01}$	$D_a = d_{01}+d_1+d_2$ $D_b = d_{01}$ $D_c = d_{01}+d_1$

①D_h and 1-D_h are the respective duty cycles of the two switching states K_h+1 and K_h for phase h (h=a, b, or c).
②For both the ascending mode (↑) and descending mode (↓), $K_aK_bK_c$ should not be the top switching state at the detected vertex.

Note that when using Table 4.2, $K_aK_bK_c$ should not be the top switching state at the detected vertex, for both the ascending (↑) and descending (↓) modes in Figure 4.8. This is easily understood because otherwise K_h+1 (h=a, b, or c) exceeds n-1.

4.2.4 Summary

Figure 4.10 gives the overall flowchart of the proposed SVM scheme. Because of the proposed mapping (Table 4.2), the encoding (for the switching states of the nearest three vectors and the respective duty cycles in each switching sequence) required by earlier SVM methods is avoided. The switching sequences are easily generated by controlling the duty cycle of each phase, which is the same procedure as for the nearest-level modulation method. Therefore, considering the extra flexibility (i.e., redundant switching states and adjustable duty cycles), the proposed scheme is more advanced than the phase-voltage modulation techniques (carrier-based modulation and nearest-level modulation), even for large level-number applications.

The switching state $K_aK_bK_c$ and the duty cycle d_{01} can be selected according to different control objectives, such as the best harmonic performance [58] [84] or the optimal capacitor voltage balancing [75] [83]. Because of the proposed mapping (Table 4.2), any achieved control objective is accompanied by the optimized switching sequences [38] [44] [58] (with the minimum number of switch transitions in every switching cycle). This feature leads to reduced switching losses and dv/dt, especially when the level number of the converter is large.

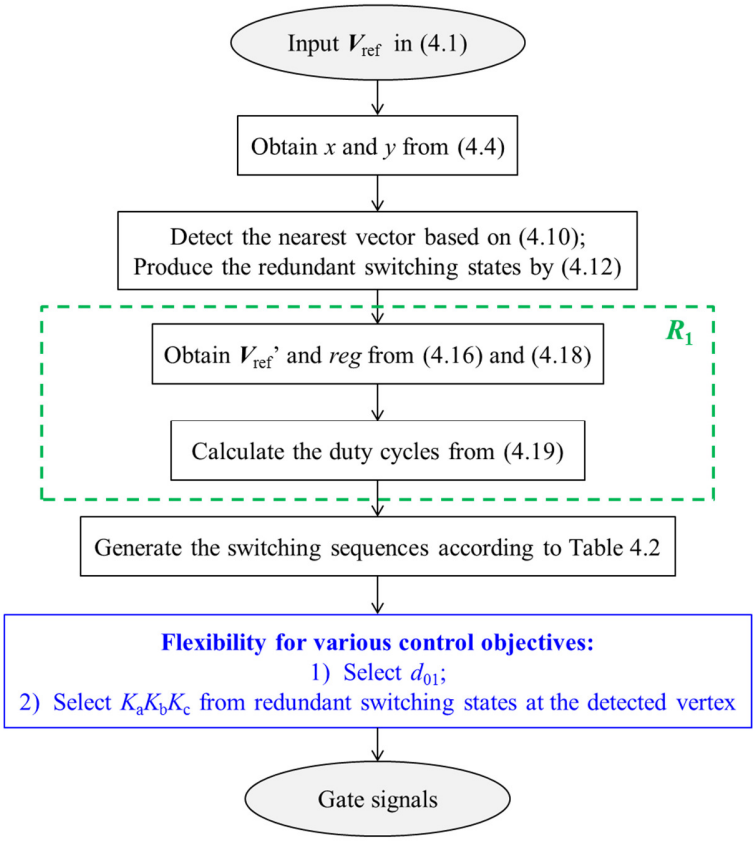


Figure 4.10 Flowchart for the proposed SVM scheme.

To avoid cross conduction during switch transitions, dead times can be added when generating the gate signals, through control software (modifying the duty cycles in Table 4.2) or gate driver hardware. Meanwhile, many compensation methods [85]-[90] can reduce voltage errors caused by the dead times and non-ideal characteristics of switching devices.

The proposed new scheme can potentially be extended to simplify the SVM for multiphase multilevel converters [62], based on the orthogonal unit-vectors introduced in Section 4.1. In multiphase applications, more redundant switching states exist [63]. A simplified scheme implies significantly reduced costs of implementation. As demonstrated in this paper for the three-phase converters, the final objective is to

implement the multiphase multilevel SVM in the same way as for the phase-voltage modulation techniques, while maintaining significant flexibility.

4.3 Simulation and Experimental Results

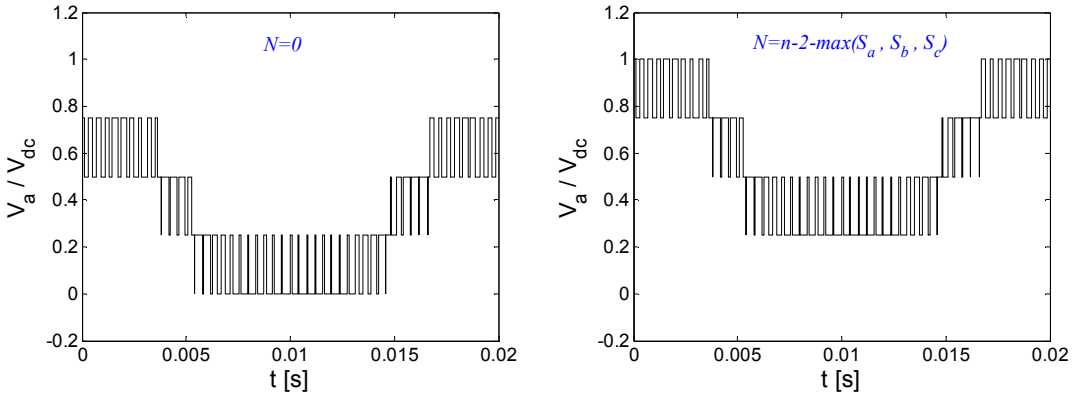
4.3.1 Simulation Results

To demonstrate the two degrees of freedom (i.e., the redundant switching sequences and the adjustable duty cycles) of the proposed new scheme, a simulation is implemented in MATLAB/Simulink for a three-phase five-level converter. In the simulation, the switching frequency is 5 kHz (fundamental frequency is 50 Hz), the modulation index is 0.6 (i.e., a low-modulation region in order to produce redundant switching states), and the switching sequence mode is changed (alternately from the ascending mode to the descending mode) after every switching cycle.

Figure 4.11 shows the simulated output voltage of phase a when $d_{01}=0.5d_0$, according to different redundant switching sequences. In Figure 4.11(a), $K_aK_bK_c$ is directly the switching state detected in (4.10). In other words, it is the bottom switching state at the detected vertex, by letting $N=0$ in (4.12). Figure 4.11(b) selects $K_aK_bK_c$ as the second top switching state at the detected vertex, i.e., $N=n$-2-max(S_a, S_b, S_c). Since different selections of $K_aK_bK_c$ lead to varied switching waveforms as in Figure 4.11, the proposed new scheme offers significant potential for optimizing the performance of a multilevel converter.

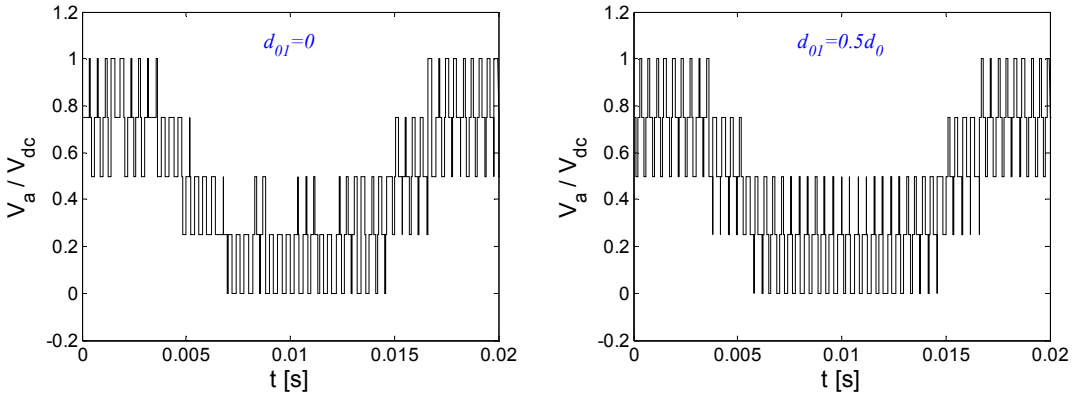
Figure 4.12 illustrates the other degree of freedom (i.e., flexible d_{01}) provided by the proposed new scheme. To represent all the possible switching states of phase a, $K_aK_bK_c$ is intentionally selected as the second top switching state at the detected vertex for the ascending mode, and as the bottom switching state for the descending mode. The waveform in Figure 4.12(a) is the voltage of phase a when $d_{01}=0$, which actually displays a discontinuous SVM pattern. It is significantly different from the voltage of phase a shown in Figure 4.12(b), where the duty cycles of the two zero vectors are equal (i.e.,

d_{01}=0.5d_0). Again, the varied switching waveforms indicate more potential for improving the performance of multilevel converters.



(a) (b)

Figure 4.11 Simulated phase *a* voltage (with respect to the negative terminal of the dc-link) according to different switching states selected for the detected vertex, when d_{01}=0.5d_0: (a) $K_aK_bK_c$ is the bottom switching state; (b) $K_aK_bK_c$ is the second top switching state.



(a) (b)

Figure 4.12 Simulated phase *a* voltage (with respect to the negative terminal of the dc-link) according to different d_{01}: (a) d_{01}=0; (b) d_{01}=0.5d_0.

4.3.2 Experimental Results

In order to verify the real-time implementation of the proposed new scheme, an experiment is carried out on a TMS320CF2812 digital signal processor (DSP). Figure 4.13 presents the schematic diagram of the experimental setup. The experiment is

implemented by running the proposed SVM algorithm on the DSP in real time for any reference vector of a three-phase five-level converter. The Code Composer Studio (CCS) [91] on a computer, which loads the compiled SVM algorithm to the DSP and starts or stops the execution of the algorithm on the DSP as needed, is applied to interface with the DSP. The DSP does not actually drive any power electronic switches, but instead sends the switching states generated by the proposed scheme to a digital-to-analog converter (DAC), which represent the phase voltages of the five-level converter as described in (8). An actual five-level converter is not required. Finally, the DAC output is measured by an oscilloscope.

The switching frequency is 1.3 kHz (fundamental frequency is 50 Hz) for the experiment, in order to highlight the switch transitions. Other operating conditions are as follows. The modulation index is 0.9 (in order to display all the voltage levels); the duty cycles of the two zero vectors are equal (i.e., d_{01}=0.5d_0); and the switching sequence mode is changed (alternately from the ascending mode to the descending mode) after every switching cycle. Figure 4.14(a) shows the simulated voltage of phase *a* (relative to the negative terminal of the dc-link) in MATLAB/Simulink for the same operating conditions. The experimental result measured from the DAC output is demonstrated in Figure 4.14(b), which is consistent with the simulation result and therefore validates the real-time implementation of the proposed new scheme.

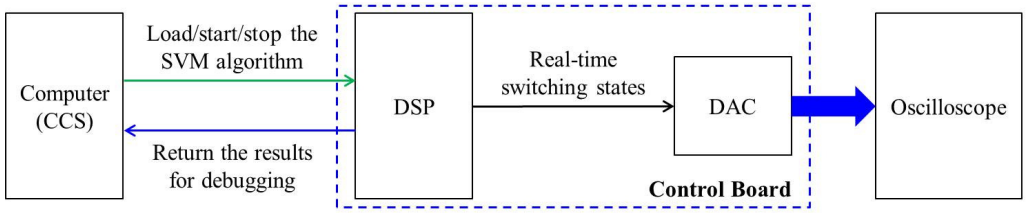
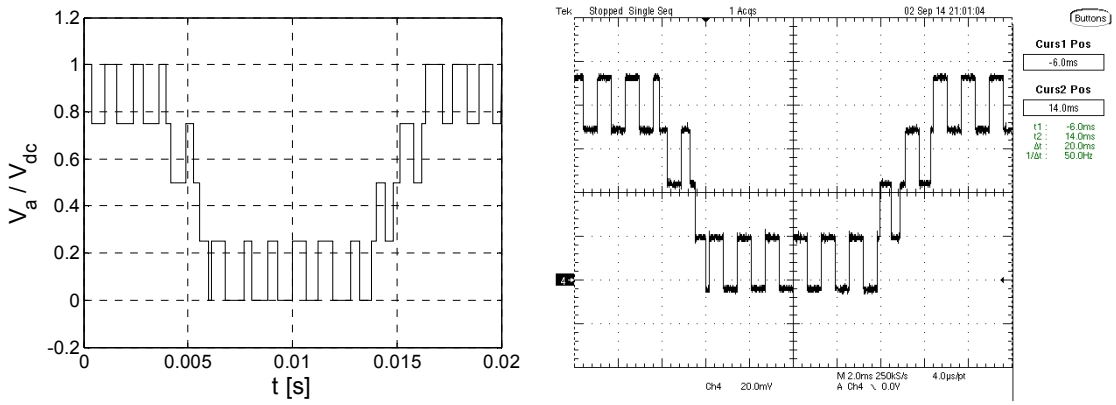


Figure 4.13 Schematic diagram of the experimental setup.



(a) (b)

Figure 4.14 Simulation and experimental results of the phase voltage (phase *a*) for a five-level converter: (a) simulated in MATLAB/Simulink; (b) measured from the DAC output, represented by the corresponding switching states generated by the proposed SVM scheme on the DSP.

4.3.3 Comparison of Real-Time Implementation

In the previous sections, some advantages of the proposed new scheme (e.g., the simplified generation of switching sequences, and the potential for multiphase multilevel applications) have been described in detail. This section further demonstrates another advantage (i.e., the superior computational efficiency), by comparing the proposed new scheme with the two typical methods introduced in [39] and [44]. Other SVM methods can be analyzed in a similar way. In Appendix A, a supplementary explanation of the methods in [39] and [44] is presented.

Based on the experimental setup in Figure 4.13, the computational times of the three SVM schemes (the proposed new scheme, the scheme in [39], and the scheme in [44]) on the DSP are compared. Table 4.2 is applied to generate the switching sequences for all the three schemes, since no method of generating the switching sequences is given in [39] and the mapping (Table 4.1) introduced in [44] is significantly simplified in the proposed new scheme (Table 4.2). In addition, the scheme in [39] is further simplified by applying the concept proposed in this paper, e.g., (4.25) and (4.27) in Appendix A. The modulation index is 0.9; the duty cycles of the two zero vectors are equal (i.e., d_{01}=0.5d_0); and the

switching sequence mode is changed (alternately from the ascending mode to the descending mode) after every switching cycle. Since the proposed new scheme and the method in [39] are independent of the level number (n) of the converter, only the result when n=5 is presented for these two schemes. On the other hand, the scheme in [44] is evaluated when n=5 and n=10.

The results in Figure 4.15 demonstrate that the proposed new scheme is computationally significantly more efficient than the method in [44], and is slightly more efficient than the method in [39]. However, compared to the method in [39], the proposed new scheme is more attractive because of the simplified rule of generating switching sequences (Table 4.2) and the potential for multiphase multilevel applications.

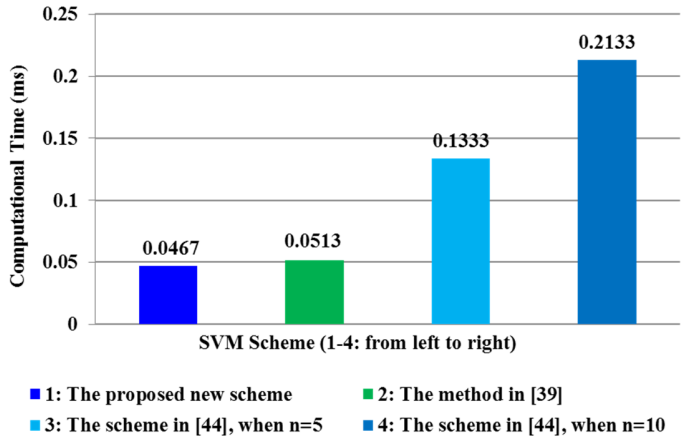


Figure 4.15 Computational times of the three SVM schemes (the proposed new scheme, the scheme in [39], and the scheme in [44]) on the DSP.

4.4 Chapter Summary

This chapter has proposed a simplified space vector modulation (SVM) scheme, for any three-phase multilevel converter. Based on two orthogonal unit-vectors that decouple the three-phase components, the proposed scheme is independent of the level number of the converter. Simulation and experimental results verify this new concept.

The proposed scheme is computationally extremely efficient. It achieves the same easy implementation as the phase-voltage modulation techniques, while maintaining the significant flexibility (i.e., redundant switching sequences and adjustable duty cycles) for optimizing the switching patterns. Therefore, it is well suited to large level-number applications. Compared with earlier SVM methods, the proposed scheme significantly simplifies the detection of the nearest three vectors and the generation of switching sequences. No lookup table or coordinate transformation is required.

This chapter has also introduced a general approach to construct the orthogonal unit-vectors for any other multiphase system. Therefore, the proposed scheme can potentially be extended to simplify the SVM for multiphase multilevel converters.

Based on the findings in Chapter 3 and this chapter, modulation methods (particularly the SVM and the nearest-level modulation) are now well suited to multilevel converters with large numbers of levels. The next chapter focuses on the power loss balancing method for three-level active neutral-point-clamped (ANPC) converters, in order to control high-power wind turbine generators and enhance the lifetimes and safe operating areas of the converters.

CHAPTER 5 IMPROVED MODULATION SCHEME FOR LOSS BALANCING OF THREE-LEVEL ACTIVE NPC CONVERTERS

As discussed in Chapters 1 and 2, the three-level neutral point clamped (NPC) converter has attracted much attention for controlling high-power wind turbine generators, but it is well-known that the NPC topology suffers from unequal power loss distribution among its semiconductor devices. The power loss unbalance problem becomes especially severe when the converter is operating at low fundamental frequencies. To overcome the loss unbalance problem of the NPC converter, the active NPC (ANPC) technique was introduced. However, it has been demonstrated [48] that in many cases, the conventional pulse width modulation (PWM) methods for the ANPC converter only marginally relieve the loss unbalance problem. Among the earlier modulation methods, the doubled frequency PWM (DF-PWM) [69] is of particular interest because it naturally doubles the apparent switching frequency (the equivalent switching frequency observed from the output voltage waveforms). The general modulation methods introduced in Chapters 3 and 4 cannot be directly applied to the ANPC converter, because for a switching state (particularly the "0" switching state as explained later) generated by those general modulation methods, the states (gate signals) of the power switches are not unique.

This chapter proposes a new modulation scheme for the three-level ANPC converter, called the adaptive DF-PWM (ADF-PWM) scheme, which significantly improves the power loss and thermal sharing among the semiconductor devices. The proposed scheme possesses the same advantage as the DF-PWM, i.e., a doubled apparent switching frequency, but offers a significantly improved power loss distribution compared with earlier modulation methods. The basic idea of the proposed scheme is adaptively adjusting the duty cycles of the switching states for every switching cycle, so as to

optimize the power loss distribution. Simulation and experimental results are presented to verify this new method.

5.1 Conventional NPC and ANPC Modulation Methods

5.1.1 NPC Converter

Figure 5.1 illustrates the circuit diagram of a three-level NPC converter [15]. The dc-link voltage V_{dc} is equally divided into two voltage sources. When the middle two switches S_{x2} and S_{x3} (x=a, b, or c) of phase x are turned on, the output terminal of the phase is clamped to the neutral point O through the diodes D_{x5} and D_{x6}. This generates an additional voltage level compared with the two-level converter.

All the switching states of the three-level NPC converter are summarized in Table 5.1, where the states "1" and "0" represent the ON and OFF states of a switch, respectively. The three switching states "P", "0", and "N", respectively, correspond to the three output voltage levels $V_{dc}/2$, 0, and $-V_{dc}/2$, with respect to the neutral point O. For each level of the output voltage v_{xO} of phase x, there is only one switching state available, so the PWM is straightforward [45]. Figure 5.2 shows the PWM waveforms for the three-level NPC converter during a switching cycle, where v_x^* is the reference voltage of phase x, and cr_1 and cr_2 are two carriers.

The reference voltages of the three phases are defined [38] as

$$v_a^* = m \cdot \frac{V_{dc}}{2}\cos(\theta) + V_{com} = v_{a1} + V_{com} \tag{5.1a}$$

$$v_b^* = m \cdot \frac{V_{dc}}{2}\cos\left(\theta - \frac{2}{3}\pi\right) + V_{com} = v_{b1} + V_{com} \tag{5.1b}$$

$$v_c^* = m \cdot \frac{V_{dc}}{2}\cos\left(\theta + \frac{2}{3}\pi\right) + V_{com} = v_{c1} + V_{com} \tag{5.1c}$$

where m is the modulation index; θ is the phase angle of the phase a voltage; V_{com} is the common-mode voltage injection; v_{x1} (x=a, b, or c) is the fundamental frequency component of v_x^*.

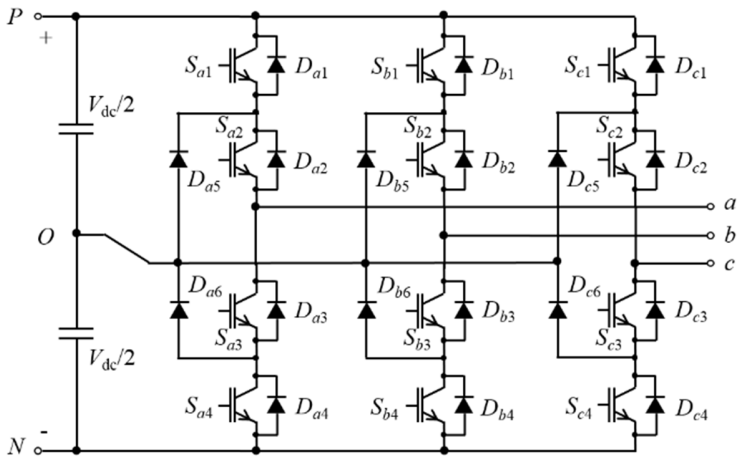
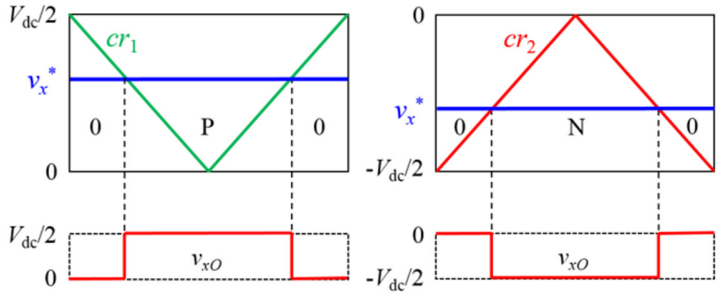


Figure 5.1 Circuit diagram of the three-level NPC converter.



(a) (b)

Figure 5.2 PWM for the three-level NPC converter: (a) $v_x^* \geq 0$; (b) $v_x^* < 0$.

Table 5.1 Switching States of the Three-Level NPC Converter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}
P	1	1	0	0
0	0	1	1	0
N	0	0	1	1

5.1.2 ANPC Converter

The three-level ANPC converter [47], as illustrated in Figure 5.3, is derived from the three-level NPC topology, by introducing the active switches S_{x5} and S_{x6} to phase x (x=a, b, or c). Together with the middle switch S_{x2} (or S_{x3}), the active switch S_{x5} (or S_{x6}) can bi-directionally control (conduct/block) the current flowing through the neutral clamping

path. Therefore, more redundant switching states are available for generating the zero output voltage.

Table 5.2 summarizes the switching states applied to the DF-PWM of the three-level ANPC converter [69]. The switching states "P" and "N" are similar to that for the NPC converter; during the "P" state the switch S_{x6} is turned on to ensure the equal voltage sharing between S_{x3} and S_{x4}, while during the "N" state the equal voltage sharing between S_{x1} and S_{x2} is guaranteed by turning on S_{x5}. Four switching states can generate the zero output voltage. The states "$0U_1$" and "$0U_2$" represent the upper neutral clamping path, i.e., the current of phase x during these two switching states is completely conducted by S_{x5}/D_{x5} and S_{x2}/D_{x2}. Similarly, the lower neutral clamping path is represented by the states "$0L_1$" and "$0L_2$", during which the current of phase x completely flows through S_{x6}/D_{x6} and S_{x3}/D_{x3}. The power losses can therefore be redistributed by selecting different neutral clamping paths.

Figure 5.4 shows the waveforms of the DF-PWM for the three-level ANPC converter. The reference voltage v_x^* of phase x in (5.1) is compared with two carriers cr_1 and cr_2 at the same time. Consequently, the generated output phase voltage v_{xO} has two notches during every switching cycle, i.e., the apparent switching frequency is doubled.

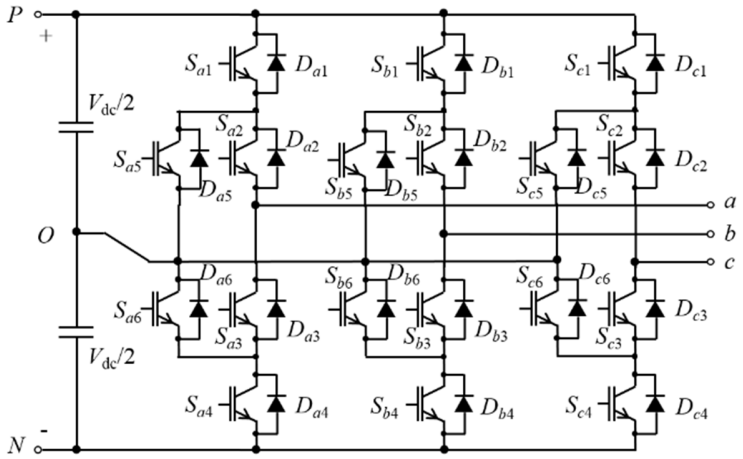
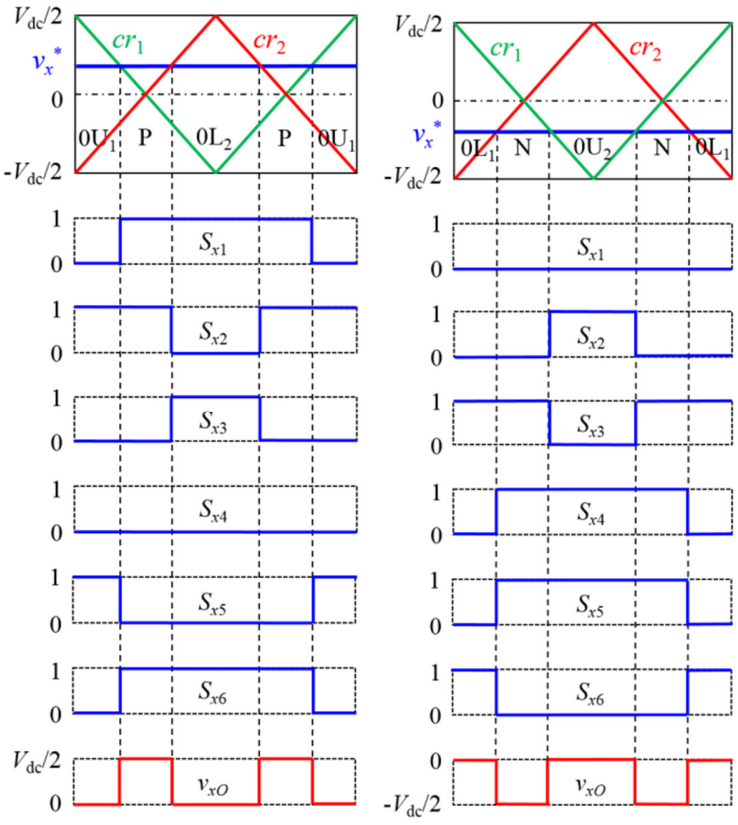


Figure 5.3 The three-level ANPC converter.



(a) (b)

Figure 5.4 DF-PWM for the ANPC converter: (a) $v_x^* \geq 0$; (b) $v_x^* < 0$.

Table 5.2 Switching States of the Three-Level ANPC Converter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}
P	1	1	0	0	0	1
$0U_1$	0	1	0	0	1	0
$0U_2$	0	1	0	1	1	0
$0L_1$	0	0	1	0	0	1
$0L_2$	1	0	1	0	0	1
N	0	0	1	1	1	0

5.2 Power Loss Unbalance of NPC and ANPC Converters

5.2.1 Loss and Thermal Analysis Method

In this paper, the loss and thermal analyses of the NPC and ANPC converters are carried out based on a numerical circuit simulation method, similar to [92]. It calculates

the power losses from the simulated instantaneous conducting current and terminal voltage of each power device.

The instantaneous conduction, turn-on, and turn-off losses of a switch are, respectively, estimated [47] [93] as

$$P_{condS} = i_s \cdot V_{fs0} + i_s^2 \cdot R_s \tag{5.2a}$$

$$P_{on} = E_{on} \cdot \frac{i_s \cdot v_{s\_pre}}{I_{s0} \cdot V_{s0}} \cdot \frac{1}{\Delta t} \tag{5.2b}$$

$$P_{off} = E_{off} \cdot \frac{i_{s\_pre} \cdot v_s}{I_{s0} \cdot V_{s0}} \cdot \frac{1}{\Delta t} \tag{5.2c}$$

where i_s and v_s are, respectively, the conducting current and terminal voltage of the switch; i_{s_pre} and v_{s_pre} are the values of i_s and v_s at the previous sampling instant, respectively; V_{fs0} is the forward voltage drop of the switch; R_s is the on-state resistance of the switch; E_{on} and E_{off} are respectively the turn-on and turn-off energies of the switch in the switching tests; I_{s0} and V_{s0} are the conducting current and blocking voltage of the switch for the switching tests; Δt is the time step of the simulator. The logics of detecting the turn-on and turn-off switching instants are, respectively, as follows:

$$\textbf{TURN} - \textbf{ON}: \ \left(i_{s\_pre} = 0\right) \text{ and } \left(v_{s\_pre} > V_{fs0} + i_{s\_pre} \cdot R_s\right) \text{ and } \left(i_s > 0\right) \tag{5.3a}$$

$$\textbf{TURN} - \textbf{OFF}: \ \left(i_{s\_pre} > 0\right) \text{ and } \left(v_s > V_{fs0} + i_s \cdot R_s\right) \text{ and } \left(i_s = 0\right) \tag{5.3b}$$

Similarly, for a diode, the instantaneous conduction and reverse recovery switching losses are, respectively, calculated [47] [93] as

$$P_{condD} = i_d \cdot V_{fd0} + i_d^2 \cdot R_d \tag{5.4a}$$

$$P_{rec} = E_{rec} \cdot \frac{i_{d\_pre} \cdot |v_d|}{I_{d0} \cdot V_{d0}} \cdot \frac{1}{\Delta t} \tag{5.4b}$$

where i_d and v_d are the conducting current and terminal voltage of the diode, respectively; V_{fd0} is the forward voltage drop of the diode; R_d is the on-state resistance of the diode; i_{d_pre} is the value of i_d at the previous sampling instant; E_{rec} is the reverse recovery energy of the diode in the switching test; I_{d0} and V_{d0} are, respectively, the conducting current and

blocking voltage of the diode for the switching test. The reverse recovery instant of the diode is detected by evaluating the following criteria:

$$\left(i_{d\_pre} > 0\right) \text{ and } \left(v_d < V_{fd0}\right) \tag{5.5}$$

The obtained total power loss of each power device (switch or diode) is fed into a thermal model [47] [94] [95], as shown in Figure 5.5, to estimate the junction temperature T_j of the device. In Figure 5.5, P_{loss} represents the total power loss of the device; $R_{th1} \sim R_{th4}$ and $C_{th1} \sim C_{th4}$ are the equivalent resistances and capacitors to form the transient thermal impedance of the device (if needed a higher-order model using more resistances and capacitors can be applied); $\tau_1 \sim \tau_4$ are the corresponding thermal time constants; T_c denotes the case temperature.

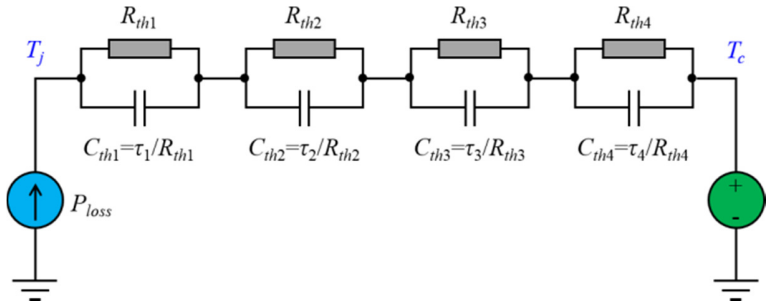


Figure 5.5 Thermal equivalent model.

5.2.2 Unbalanced Power Losses of NPC and ANPC Converters

The unbalanced loss distribution of the NPC and ANPC converters is demonstrated based on the conditions in Table 5.3. The FF225R17ME4 insulated-gate bipolar transistor (IGBT) with an anti-parallel diode [96], whose parameters are listed in Table B.1 in Appendix B, is selected as an example for the power devices. Since the DF-PWM naturally doubles the apparent switching frequency, the switching/carrier frequency of the ANPC converter (1 kHz) is 50% of that of the NPC converter (2 kHz). A zero common-mode voltage is applied for demonstration purposes, i.e., V_{com}=0 in (5.1).

Table 5.3 Test Condition for the NPC and ANPC Converters

Parameter	Value
RMS current (I_{rms})	225 A (50 Hz or 10 Hz)
Power factor (pf)	0.8
DC-link voltage (V_{dc})	1070 V
Carrier frequency (f_s)	1 kHz (ANPC) or 2 kHz (NPC)
Modulation index (m)	0.8
Simulation time step (Δt)	4 μs
Power device	FF225R17ME4 IGBT/Diode
Case temperature (T_c)	100 °C

Figure 5.6 shows the average power losses for the power devices of the NPC and ANPC converters, when the fundamental frequency is 50 Hz. Only half of the power devices in each phase are presented since the two arms of each phase are symmetrical. Compared to the NPC converter, the ANPC converter only influences the current paths for the zero output voltage, so the conduction losses of S_{x1}/D_{x1} (S_{x4}/D_{x4}) for the two converters are almost identical if the same reference voltages are applied. However, the ANPC converter reduces the switching loss of S_{x1}/D_{x1} (S_{x4}/D_{x4}) because of the lower switching frequency. This is a significant advantage of the DF-PWM.

It is also shown in Figure 5.6 that by controlling the neutral clamping current paths, the ANPC converter redistributes the power losses of S_{x2}/D_{x2} (S_{x3}/D_{x3}) and S_{x5}/D_{x5} (S_{x6}/D_{x6}). However, the improvement on the loss balancing is very limited; S_{x2} (S_{x3}) still brings about much larger power loss than the other devices under the test condition. A similar conclusion can be obtained for other operating conditions of the converters, by analysis analogous to [47]. The most stressed device is further challenged by low fundamental frequency operating conditions (e.g., the rotor side converter of DFIG systems), though the fundamental frequency does not influence the average power losses (average junction temperatures) of the devices. For example, Figure 5.7 shows the instantaneous junction temperatures of the most stressed device S_{x2} under the test condition for the NPC and ANPC converters, at two different fundamental frequencies (50 Hz and 10 Hz). Larger ripples of the junction temperatures occur at the lower

fundamental frequency, which further undermine the lifetimes of the devices. Therefore, the selection of the neutral clamping current paths needs to be optimized.

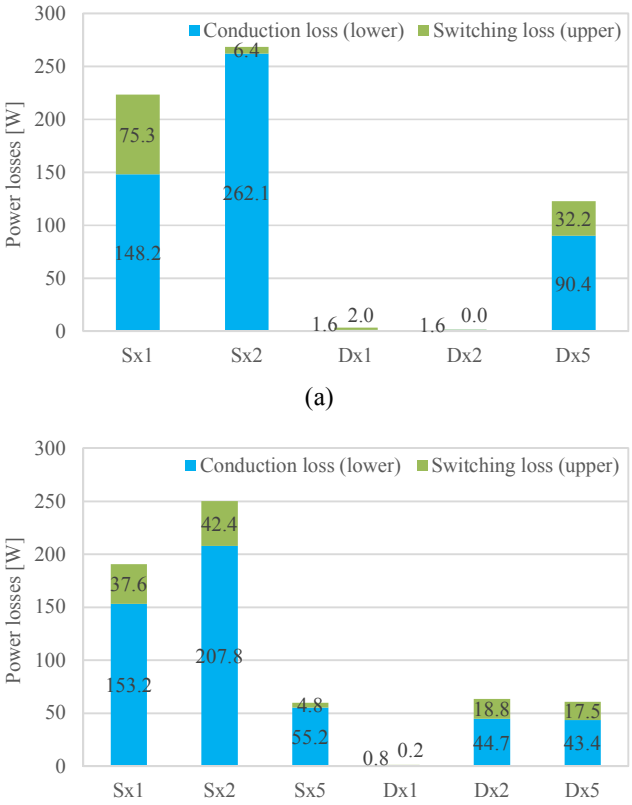


Figure 5.6 Loss distribution of NPC and ANPC converters using conventional modulation schemes: (a) NPC converter; (b) ANPC converter.

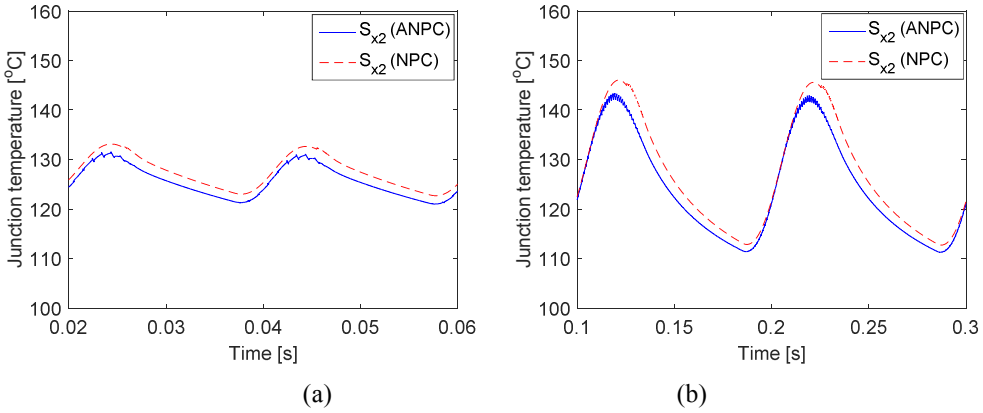


Figure 5.7 Junction temperatures of S_{x2} for NPC and ANPC converters using conventional modulation, at different fundamental frequencies: (a) 50 Hz; (b) 10 Hz.

5.3 ADF-PWM for the ANPC Converter

5.3.1 Modulation Strategy

The ANPC converter offers the following two degrees of freedom to balance the power losses, as aforementioned: 1) for S_{x1}/D_{x1} (S_{x4}/D_{x4}), the switching loss can be reduced by applying a lower switching frequency while not affecting the apparent switching frequency; 2) the losses of S_{x2}/D_{x2} (S_{x3}/D_{x3}) and S_{x5}/D_{x5} (S_{x6}/D_{x6}) can be redistributed by appropriately selecting the redundant "0" switching states. Accordingly, this paper proposes a new modulation scheme for the ANPC converter, called the ADF-PWM. It possesses the same advantage as the DF-PWM, i.e., a doubled apparent switching frequency, but offers a significantly improved loss distribution.

The proposed modulation scheme is explained as follows, taking the reference voltage $v_x^*>0$ as an example. Table 5.4 summarizes the switching states utilized in the proposed scheme; a new switching state "0UL" turns on both the upper and lower neutral clamping paths. Since $v_x^*>0$, the switching states for the switching cycle are composed of "P" and appropriate "0" states. At first, it is observed from Figure 5.4(a) that S_{x2}/D_{x2} generates the maximum loss among all the devices of phase x because S_{x2}/D_{x2} is ON for the switching state "P". In order to control/reduce the power loss of S_{x2}/D_{x2}, a "0" switching state ("$0L_1$" or "$0L_2$"), for which S_{x2}/D_{x2} is OFF, needs to be selected. Another "0" state, i.e., "$0U_1$" or "$0U_2$", is then applied to make the conduction periods of S_{x2}/D_{x2} and S_{x3}/D_{x3} (S_{x6}/D_{x6}) equal.

Table 5.4 Switching States of the ADF-PWM for the ANPC Converter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}
P	1	1	0	0	0	1
$0U_1$	0	1	0	0	1	0
$0U_2$	0	1	0	1	1	0
0UL	0	1	1	0	1	1
$0L_1$	0	0	1	0	0	1
$0L_2$	1	0	1	0	0	1
N	0	0	1	1	1	0

Figure 5.8 illustrates two modulation modes according to the above analysis. For mode 1 shown in Figure 5.8(a), the outer device S_{x1}/D_{x1} and clamping device S_{x5}/D_{x5} undertake the major switching stresses; the other devices operate at so-called "soft switching" (highlighted by dashed circles) conditions because of the switching state "0UL". The switching state "0UL" is called a "transition state" and is only used for generating the aforementioned soft switching, so its duty cycle can be very small as long as it is large enough for the devices' switching transients. Neglecting the duty cycle of the transition state, the conduction periods of S_{x2}/D_{x2} and S_{x3}/D_{x3} (S_{x6}/D_{x6}) are both half of the switching cycle T_s. In other words, the power losses among S_{x2}/D_{x2}, S_{x3}/D_{x3}, S_{x5}/D_{x5}, and S_{x6}/D_{x6} are maximally balanced for every switching cycle. Similarly, Figure 5.8(b) shows the other modulation mode (mode 2), where the inner devices S_{x2}/D_{x2} and S_{x3}/D_{x3} undertake the major switching stresses. Two transition states "$0L_2$" and "0UL" are applied to operate the other devices at soft switching (highlighted by dashed circles).

It is observed from Figure 5.8 that v_x^* needs to be less than $V_{dc}/4$ to maintain the conduction period of S_{x2}/D_{x2} (S_{x3}/D_{x3}) as $T_s/2$. When v_x^* is larger than $V_{dc}/4$, the upper neutral clamping path is eliminated to reduce the power loss of S_{x2}/D_{x2} because now S_{x2}/D_{x2} always has a larger duty cycle than S_{x3}/D_{x3}. Figure 5.9 illustrates two modulation modes when $v_x^*>V_{dc}/4$, similar to Figure 5.8. The outer device S_{x1}/D_{x1} and clamping device S_{x5}/D_{x5} undertake the major switching stresses for mode 1 shown in Figure 5.9(a), where two transition states "$0U_1$" and "0UL" are applied. For mode 2 shown in Figure 5.9(b), the inner devices S_{x2}/D_{x2} and S_{x3}/D_{x3} undertake the switching stresses.

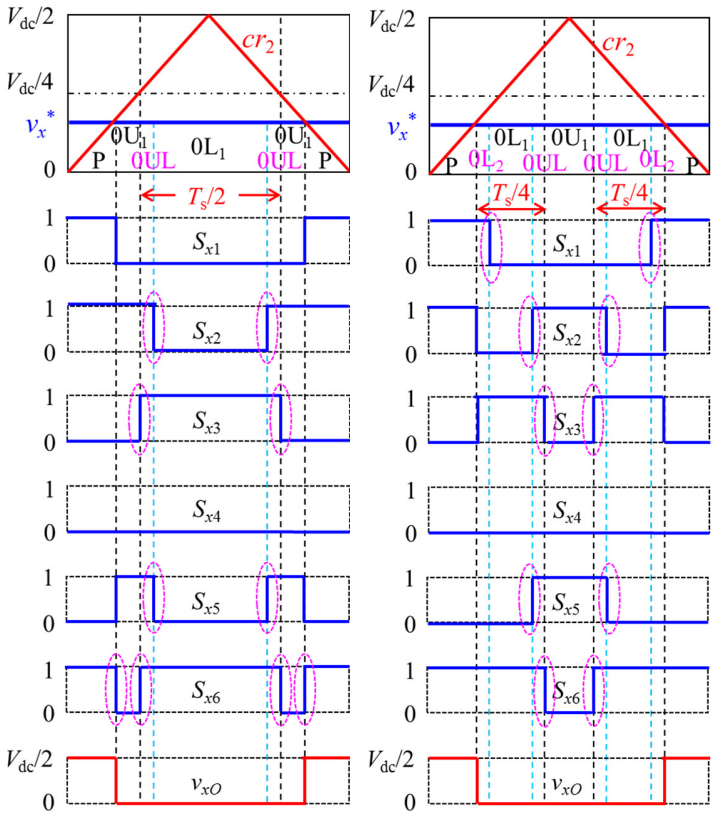


Figure 5.8 Two PWM modes when $0 \le v_x^* \le V_{dc}/4$: (a) mode 1; (b) mode 2.

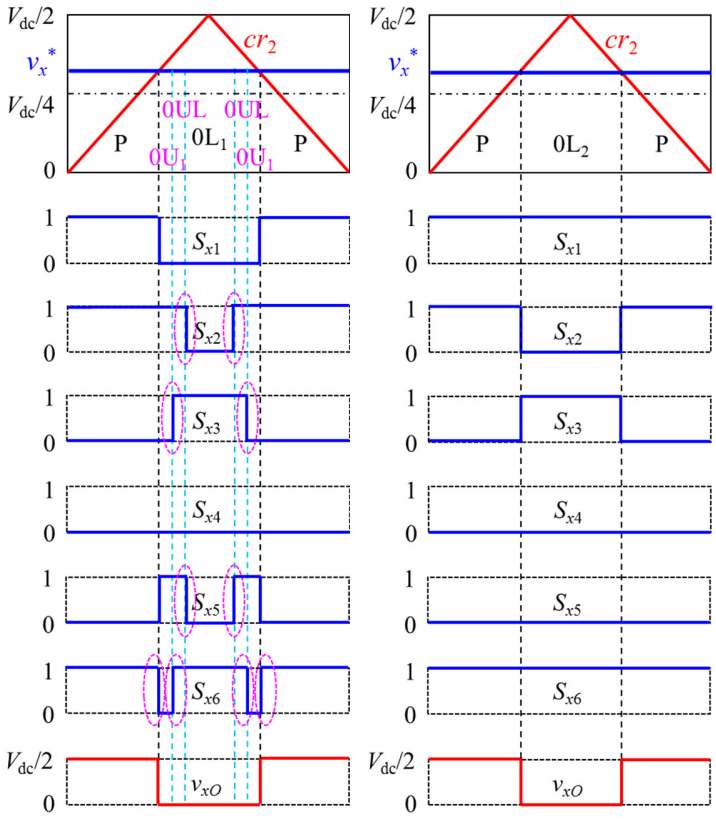


Figure 5.9 Two PWM modes when $v_x^* > V_{dc}/4$: (a) mode 1; (b) mode 2.

The proposed ADF-PWM modulation scheme for the ANPC converter is illustrated in Figure 5.10, where the frequency of the carrier *cr* is $1/T_s$. To double the apparent switching frequency, the aforementioned two modulation modes are combined for each case. For example, Figure 5.10(a) combines the two modulation modes shown in Figure 5.8. The mode 1 is highlighted by a dashed circle, while the other switching states are obtained from the mode 2. The required duty cycles are as follows:

$$d_{\mathrm{P}} = 2|v_x^*|/V_{dc} \tag{5.6a}$$

$$d_{0\mathrm{U1}} = 0.5 - d_{\mathrm{P}} \tag{5.6b}$$

$$d_{\mathrm{t}} = 2T_{\mathrm{t}}/T_{\mathrm{s}} \tag{5.6c}$$

where $|v_x^*|$ is the absolute value of v_x^*; T_t represents the conduction period of each transition state. In this paper, T_t=4 μs is selected for demonstration purposes.

Similarly, Figure 5.10(b) combines the two modulation modes shown in Figure 5.9. The duty cycles are obtained as follows:

$$d_{0L2} = 0.5(1 - d_P) \tag{5.7}$$

and d_P and d_t are the same as in (5.6).

Analogous analyses can be carried out for $v_x^* \leq 0$. Figure 5.10(c) and (d) are symmetrical to Figure 5.10(a) and (b), respectively. The corresponding duty cycles for Figure 5.10(c) and (d) are, respectively, obtained from (5.6) and (5.7).

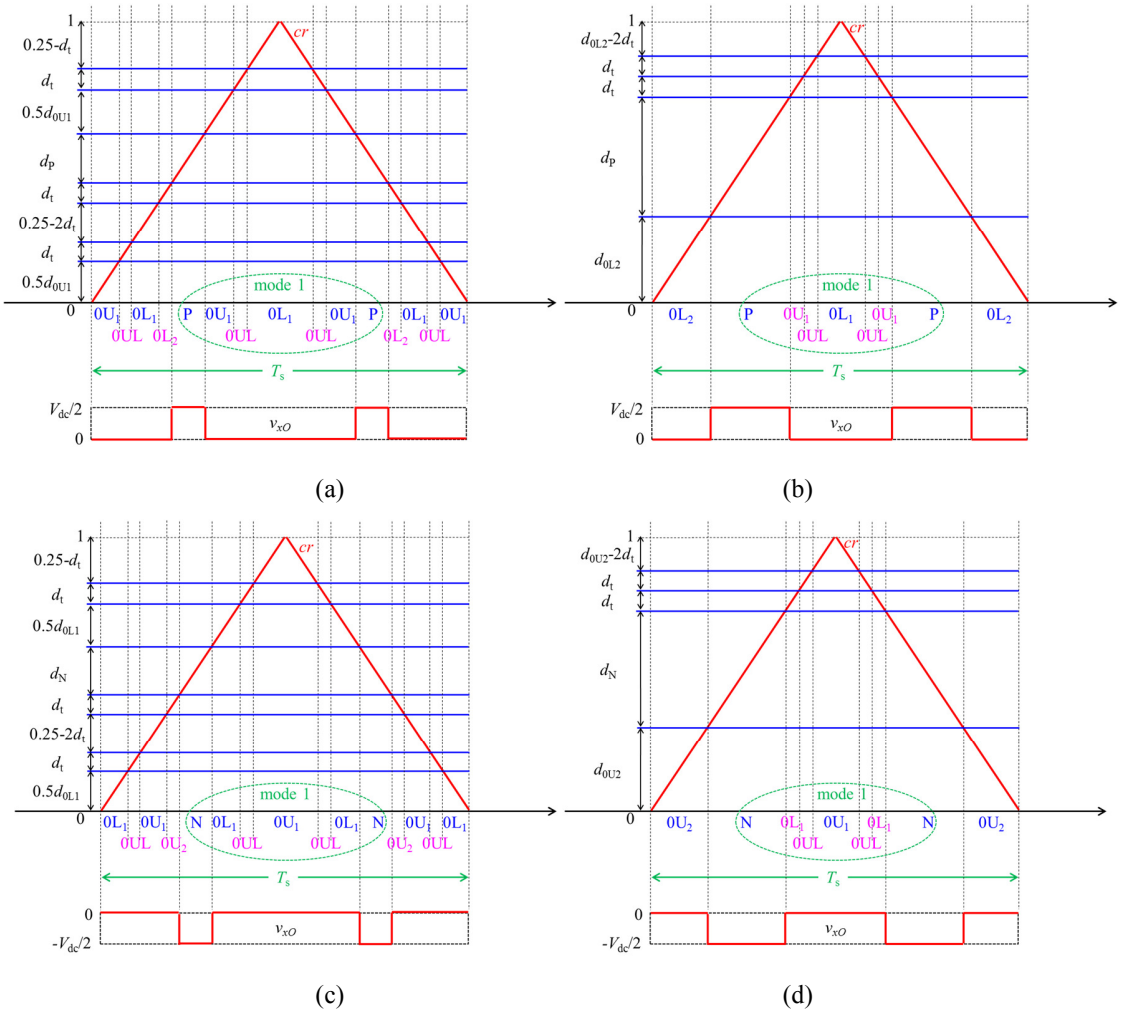


Figure 5.10 Proposed ADF-PWM modulation scheme for the ANPC converter: (a) $0 \leq v_x^* \leq V_{dc}/4$; (b) $v_x^* > V_{dc}/4$; (c) $-V_{dc}/4 \leq v_x^* < 0$; (d) $v_x^* < -V_{dc}/4$.

Note that though the proposed ADF-PWM strategy is demonstrated according to carrier-based modulation, it can also be conveniently applied to other modulation schemes (e.g., space-vector modulation [44] [97] and nearest-level modulation [38]), because of the equivalence among the various modulation methods [38]. For example, if a switching sequence d_{01}*$S_{a01}S_{b01}S_{c01} \rightarrow d_1$*$S_{a1}S_{b1}S_{c1} \rightarrow d_2$*$S_{a2}S_{b2}S_{c2} \rightarrow d_{02}$*$S_{a02}S_{b02}S_{c02}$ is generated by the space-vector modulation for a reference vector, then the switching sequence can be equivalently achieved [38] [97] by applying the following reference voltage of phase x (x=a, b, or c) to the ADF-PWM

$$v_x^* = (d_{01}S_{x01} + d_1S_{x1} + d_2S_{x2} + d_{02}S_{x02} - 1)V_{dc}/2 \tag{5.8}$$

where d_{01}, d_1, d_2, and d_{02} are the duty cycles of the four switching states $S_{a01}S_{b01}S_{c01}$, $S_{a1}S_{b1}S_{c1}$, $S_{a2}S_{b2}S_{c2}$, and $S_{a02}S_{b02}S_{c02}$, respectively; any switching state (S_{x01}, S_{x1}, S_{x2}, or S_{x02}) of phase x is among $\{0, 1, 2\}$.

In addition, the ADF-PWM strategy is demonstrated based on assuming identical switching characteristics of the power devices. If the power devices have different switching characteristics, the duty cycles in (5.6) and (5.7) can be adjusted accordingly to optimize the power loss balancing. For instance, increasing d_{0U1} in (5.6) and reducing the duty cycle of "$0L_1$" at the same time can compensate for the difference between the switching energies of S_{x2}/D_{x2} and S_{x3}/D_{x3}, if the switching energy of S_{x3}/D_{x3} is larger than that of S_{x2}/D_{x2}. It should be noted that at low switching frequencies (i.e., normal operating conditions of the ANPC converter in medium-voltage high-power applications) conduction losses dominate the power losses of the power devices, so different switching energies of the power devices will not cause significant adjustments to the duty cycles in (5.6) and (5.7).

To avoid cross conduction during switch transitions, dead times can be added when generating the gate signals, through control software (modifying the duty cycles) or gate driver hardware. The dead times (2 μs in this paper) should be smaller than the conduction periods of the transition states.

5.3.2 Optimized Common-Mode Voltage Injection

According to Figures 5.8 and 5.9, it is easier for the ANPC converter to balance the power losses when the reference voltage v_x^* is within the range [-V_{dc}/4, V_{dc}/4]; the conduction loss of S_{x1}/D_{x1} (S_{x4}/D_{x4}) can only be controlled by adjusting the reference voltage. Therefore, when the modulation index m is larger than 0.5, the common-mode voltage V_{com} in (5.1) can be adjusted as follows to further improve the loss balancing.

An objective function is defined accordingly:

$$J = \sum_{x=a,b,c}[(v_{x1} + V_{com})^2 \cdot i_x^2] \tag{5.9}$$

where i_x (x=a, b, or c) is the instantaneous current of phase x; v_{x1} is the instantaneous value of the fundamental frequency component of v_x^* as in (5.1). The current of each phase is considered as the weighing factor, since a larger current (absolute value) enlarges the power loss unbalance between S_{x2}/D_{x2} and S_{x3}/D_{x3} as explained for Figure 5.9. By minimizing the objective function, the reference voltage (absolute value) for the phase with the maximum current is adjusted to the smallest value.

The general solution to minimize the objective function is

$$V_{com} = -\sum_{x=a,b,c}(v_{x1} \cdot i_x^2) \,/\, \sum_{x=a,b,c} i_x^2 \tag{5.10}$$

which needs to be limited to the range [-V_{dc}/2-min(v_{a1}, v_{b1}, v_{c1}), V_{dc}/2-max(v_{a1}, v_{b1}, v_{c1})], where min(v_{a1}, v_{b1}, v_{c1}) and max(v_{a1}, v_{b1}, v_{c1}) denote the minimum and maximum values among v_{a1}, v_{b1}, and v_{c1}, respectively.

It is well-known that for a stand-alone ANPC (same as NPC) converter, the common-mode voltage is normally utilized to balance the dc-link capacitor voltages [38] [83] [98], so in this condition (5.10) is no longer applicable. However, for a back-to-back configuration of ANPC converters (such as in WECSs), only one ANPC converter (the grid side converter) is responsible for capacitor voltage balancing, and therefore the other ANPC converter (the machine side converter) can apply (5.10) to optimize the power loss distribution. This is particularly useful since the machine side converter is under heavier

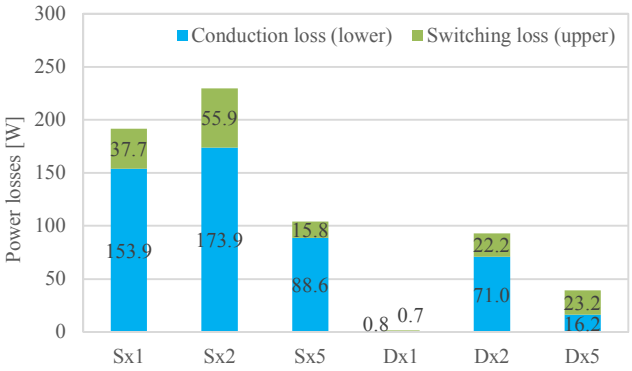
thermal stress than the grid side converter, because of the lower fundamental frequency operating conditions as explained previously.

5.4 Simulation Results

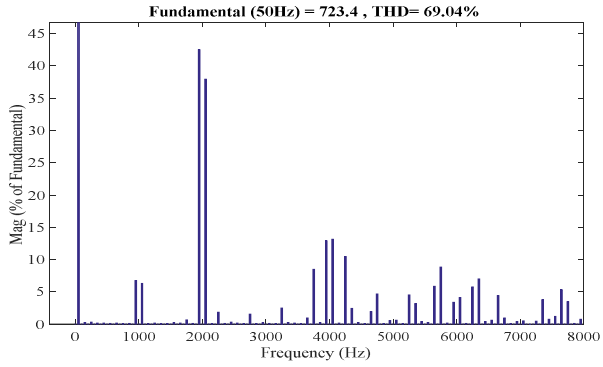
5.4.1 Comparison with Conventional Modulation Method

Figure 5.11 shows the loss distribution of the ANPC converter and harmonic spectrum of the output voltage v_{ab} (phase *a* to phase *b*) for the test conditions in Table 5.3, using the ADF-PWM when the common-mode voltage is V_{com}=0. The harmonic spectrum demonstrates that a doubled apparent switching frequency (2 kHz) is achieved. Compared to the results in Figure 5.6, the ADF-PWM thus further improves the loss balancing by reducing the power loss of the most stressed devices (S_{x2} and S_{x3}). It is also observed that the switching loss of S_{x2} is slightly increased compared to using the DF-PWM. This is because the "soft switching" events resulting from the transition states still cause some switching losses. However, as explained previously, the increased switching loss is much smaller than the reduction of the conduction loss.

The instantaneous junction temperatures of the most stressed device S_{x2} for the NPC and ANPC converters appear in Figure 5.12, which shows that the ADF-PWM method significantly reduces the peak and ripple of the junction temperature. When the fundamental frequency is lower (10 Hz), the improvement resulting from the ADF-PWM is more significant. Table B.2 in Appendix B summarizes the average, peak, and ripple (peak-to-peak) of the junction temperatures for Figure 5.12.

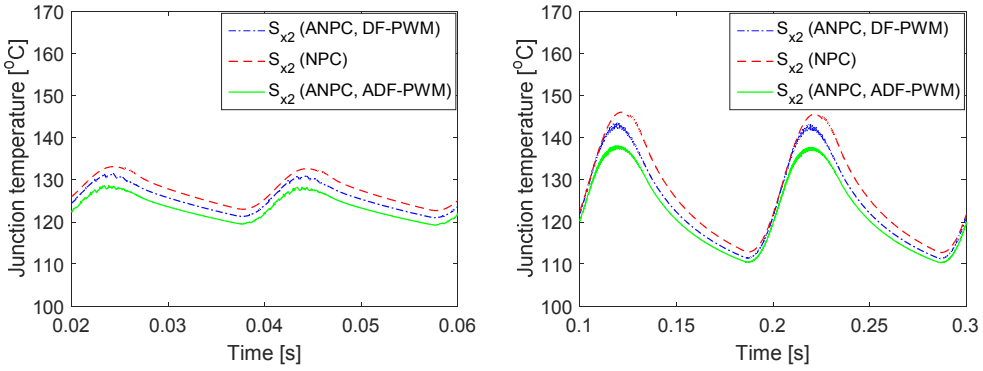


(a)



(b)

Figure 5.11 Loss distribution of the ANPC converter and harmonic spectrum of v_{ab}, using the ADF-PWM: (a) loss distribution; (b) harmonic spectrum.



(a) (b)

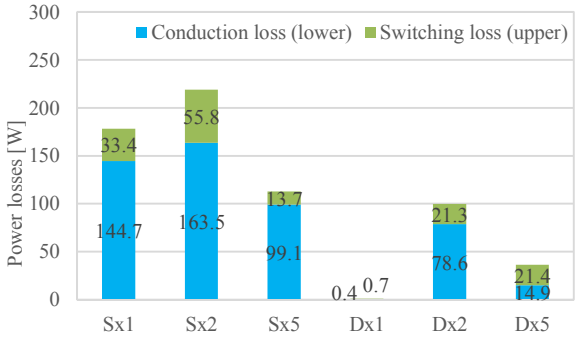
Figure 5.12 Junction temperatures of S_{x2} for NPC and ANPC converters (when different modulation schemes are used) at different fundamental frequencies: (a) 50 Hz; (b) 10 Hz.

5.4.2 Effectiveness of the Optimized Common-Mode Voltage

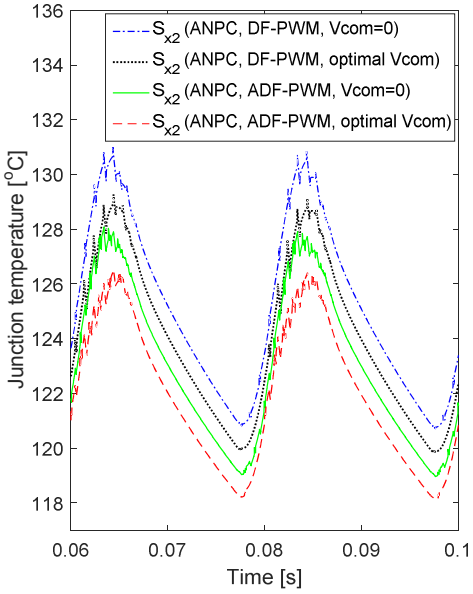
Based on the test conditions in Table 5.3, Figure 5.13(a) presents the loss distribution of the ANPC converter using the ADF-PWM, when the optimized common-mode voltage in (5.10) is applied. The power loss of the most stressed devices (S_{x2} and S_{x3}) is further reduced, compared with the results in Figure 5.11; the power loss of S_{x1}/D_{x1} (S_{x4}/D_{x4}) is also changed/reduced because of the adjusted common-mode voltage.

Figure 5.13(b) shows the instantaneous junction temperature of the most stressed device (S_{x2}) under the aforementioned test conditions, when the fundamental frequency is 50 Hz. The optimized common-mode voltage further reduces the peak junction temperature (from 128 ºC to 126 ºC). The average, peak, and ripple (peak-to-peak) of the junction temperatures for Figure 5.13 are summarized in Table B.3 in Appendix B.

Figure 5.14 compares the total power losses (50% of one phase leg) of the ANPC converter, for different modulation schemes and different common-mode voltages. The ADF-PWM optimizes the power loss balancing among the power devices, but slightly increases the total power loss of the ANPC converter (due to the "soft switching" events). The optimized common-mode voltage in (5.10) reduces the total power loss of the ANPC converter for both the DF-PWM and ADF-PWM schemes.



(a)



(b)

Figure 5.13 Results of the ADF-PWM for the ANPC converter, when the optimized V_{com} is applied: (a) loss distribution; (b) junction temperatures of S_{x2}.

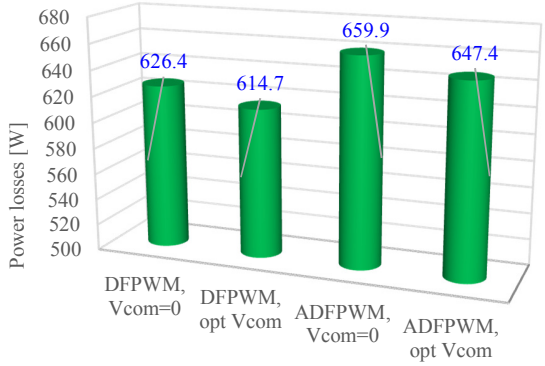


Figure 5.14 Total power losses of the ANPC converter, for different modulation schemes and different common-mode voltages.

5.5 Experimental Results

The proposed ADF-PWM modulation scheme is also tested based on the experimental setup shown in Figure 5.15 and the operating conditions summarized in Table 5.5. Since the three phases of the ANPC converter are symmetric, only a single phase x (x=a, b, or c) is constructed; the load (resistor and inductor) is connected between the node x in Figure 5.3 and the neutral point O. Two DC power supplies serve as the two voltage sources and both maintain 80 V dc-link voltages. A real-time simulator OPAL-RT [99] is used to run the ADF-PWM scheme in real time and to generate the gate signals for the ANPC converter. The OPAL-RT interfaces (receives commands and sends real-time results) with a command station (laptop) via TCP/IP protocol. A thermal imaging camera is used to monitor the thermal dynamics.

Figure 5.16 shows the measured output voltage v_{xO} and current (represented by the voltage of the load resistor) of the ANPC converter, for each of the ADF-PWM and DF-PWM schemes. The output voltages for the two modulation schemes are identical, and a doubled apparent switching frequency (2 kHz) can be observed by counting the number of pulses for each fundamental cycle of the output voltage waveform, or by carrying out a harmonic analysis similar to Figure 5.11(b). The gate signals ($\bar{S}_{x1}$ and $\bar{S}_{x2}$) generated by the OPAL-RT for the switches S_{x1} and S_{x2} also appear in Figure 5.16, which clearly demonstrate different switching patterns. Note that in the gate driver circuits, $\bar{S}_{x1}$ and $\bar{S}_{x2}$ are inverted before being sent to the switches. The thermal images in Figure 5.17 compare the thermal performances of the ADF-PWM and DF-PWM schemes. The ADF-PWM leads to a lower maximum junction temperature (77.7 ºC) than that caused by the DF-PWM (80.6 ºC).

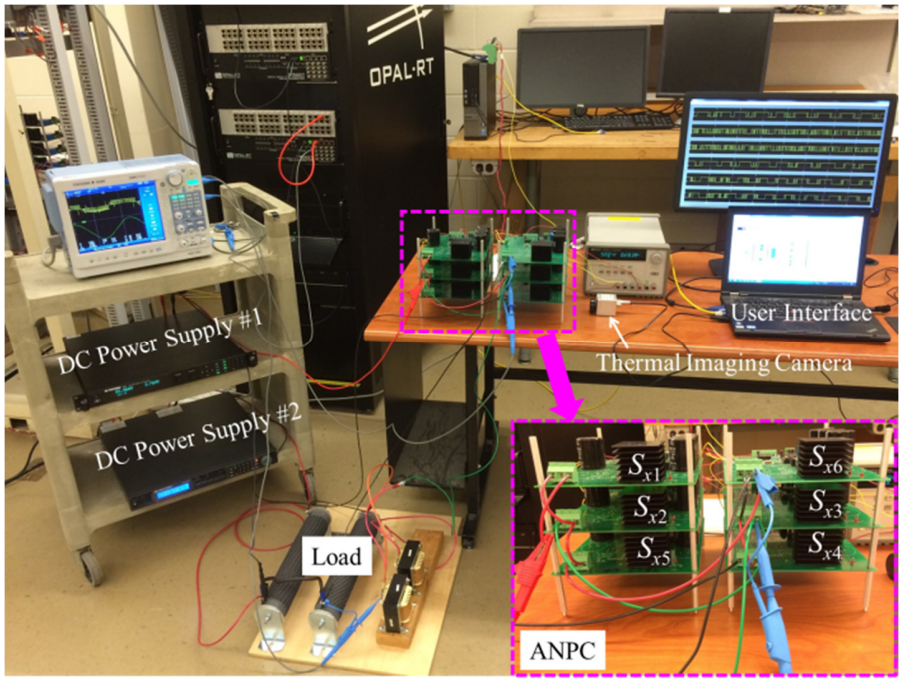
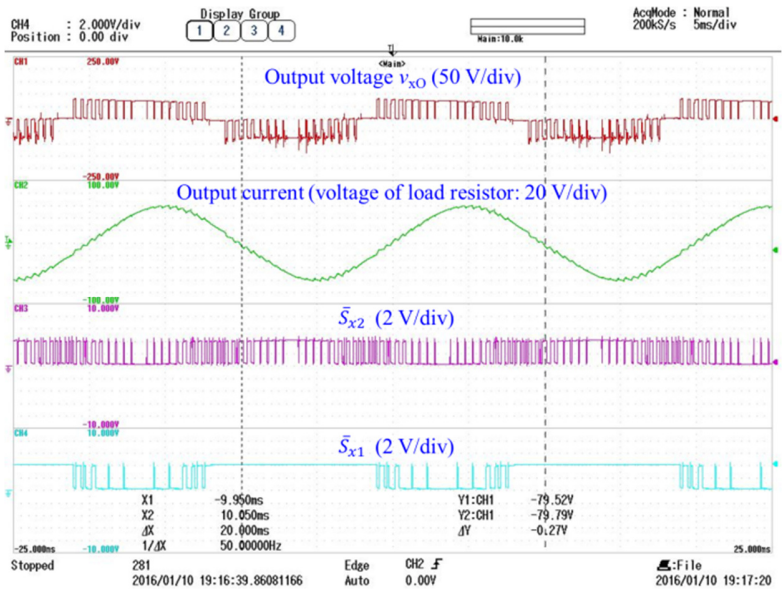


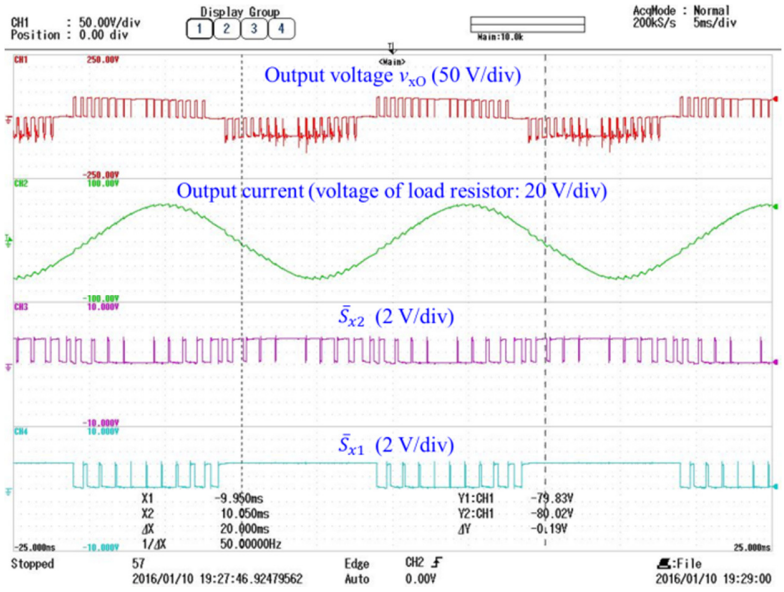
Figure 5.15 Experimental setup.

Table 5.5 Test Condition for the Experiment

Parameter	Value
DC-link voltage (V_{dc})	160 V
Carrier frequency (f_s)	1 kHz
Modulation index (m)	1.0
Load resistance and inductance	3 Ω + 5 mH
Fundamental frequency (f_0)	50 Hz
OPAL-RT time step (Δt)	8 μs
Conduction period of transition state (T_t)	8 μs
Power device	IXYS FII 40-06D IGBT/Diode
Ambient temperature (T_a)	25 °C

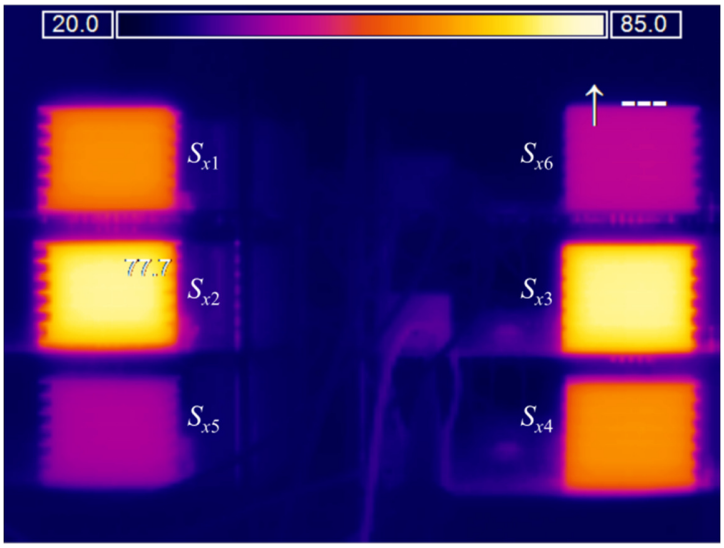


(a)

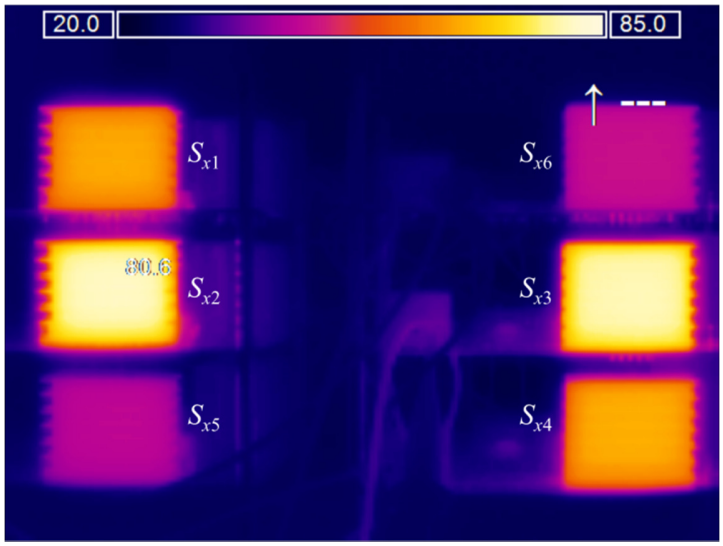


(b)

Figure 5.16 Experimental waveforms of the ANPC converter for two modulation schemes: (a) ADF-PWM; (b) DF-PWM.



(a)



(b)

Figure 5.17 Thermal experimental results for two modulation schemes: (a) ADF-PWM; (b) DF-PWM.

5.6 Chapter Summary

This chapter has introduced a new modulation scheme, called the ADF-PWM, for the three-level ANPC converter. It possesses the same advantage as the DF-PWM, i.e., a doubled apparent switching frequency, but offers a significantly improved power loss distribution and thermal dynamic. The basic idea of the proposed scheme is adaptively adjusting the duty cycles of the switching states for every switching cycle, so as to

optimize the power loss distribution. Simulation and experimental results verify this new concept.

A general approach, to inject an optimized common-mode voltage for loss balancing, has also been presented. The optimized common-mode voltage further improves the performance of the ADF-PWM.

This chapter has also investigated the influence of the fundamental frequency on the thermal dynamics of the NPC and ANPC converters. It is demonstrated that low fundamental frequencies further aggravate the converters' power loss and junction temperature unbalance. Since the proposed ADF-PWM scheme optimizes the power loss distribution for every switching cycle, both average and instantaneous/peak junction temperatures of the most stressed semiconductors are reduced by the ADF-PWM scheme (compared with the conventional modulation method for the ANPC converter), especially at low fundamental frequencies.

Since in this chapter the control of the ANPC converter for a single wind turbine generator has been solved, the next chapter revolves around the control of the modular multilevel converter (MMC), which is crucial to wind energy high voltage direct current (HVDC) transmission for large wind farms.

CHAPTER 6 OPTIMIZED CONTROL OF THE MODULAR MULTILEVEL CONVERTER BASED ON SPACE VECTOR MODULATION

Chapter 5 has solved the control of the active neutral-point-clamped (ANPC) converter for a single wind turbine generator. For high voltage direct current (HVDC) energy transmission of large wind farms, the modular multilevel converter (MMC) is the best choice as discussed in Chapters 1 and 2.

This chapter presents a general space vector modulation (SVM) method for the MMC, based on the SVM scheme introduced in Chapter 4. Compared with earlier modulation methods for the MMC, the proposed SVM method not only generates the maximum level number (i.e., $2n+1$, where n is the number of submodules in the upper or lower arm of each phase) of the output phase voltages, but also leads to an optimized control performance in terms of capacitor voltage balancing and circulating current suppression. The maximum level number is achieved by introducing a new equivalent circuit of the MMC, and the optimized control is obtained by selecting the optimal redundant switching states. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed method is well suited to the MMC with any number of submodules (SMs). Simulation and experimental results are presented to validate the proposed method.

6.1 Equivalent Circuit and Control of the MMC

6.1.1 Equivalent Circuit of the MMC

Figure 6.1 shows the circuit diagram of one phase (phase *a*) of the MMC, which contains an upper arm and a lower arm. There are n SMs in each arm (i.e., SM_{aP1}-SM_{aPn} in the upper arm and SM_{aN1}-SM_{aNn} in the lower arm), and a detailed half-bridge

submodule (SM) is shown in Figure 6.1. The output voltage v_{SM} of a SM is v_C ("ON" state) when S_1 is switched on and S_2 is switched off, and is zero ("OFF" state) when S_1 is switched off and S_2 is switched on. V_{dc} and i_{dc} are respectively the dc-link voltage and current; i_{ap} and i_{an} are the currents of the upper and lower arms, respectively; and i_a is the output current of phase *a*. The inductors (inductance is L_0) in the upper and lower arms are the buffer inductors; the parasitic ohmic losses in each arm are represented by a resistor R_0. Other phase legs are identical to phase *a*.

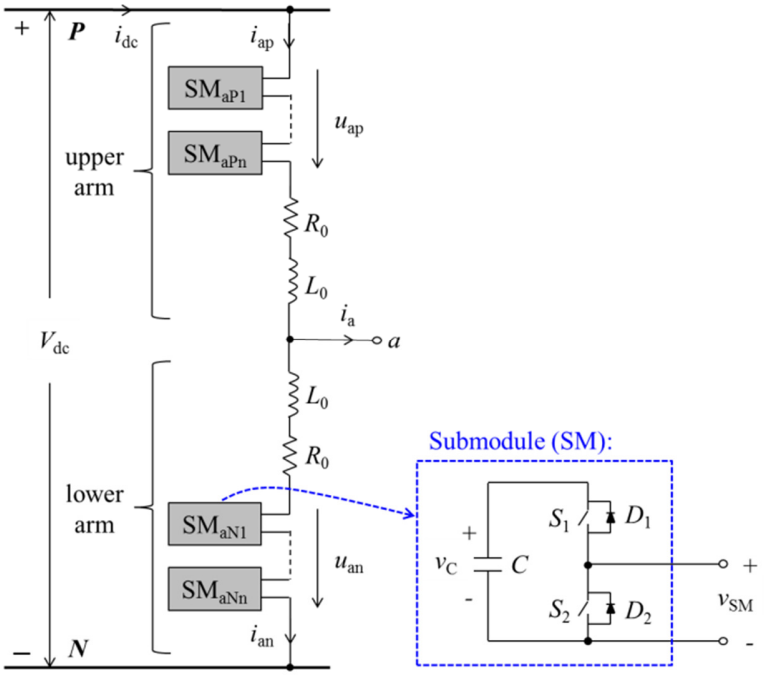


Figure 6.1 Circuit diagram of one phase of the MMC.

Based on Kirchhoff's voltage law, the output voltage v_a of phase *a* relative to the negative terminal of the dc-link is respectively calculated for the upper and lower arms as follows

$$v_a = V_{dc} - u_{ap} - L_0 \cdot di_{ap}/dt - R_0 \cdot i_{ap} \tag{6.1a}$$

$$v_a = u_{an} + L_0 \cdot di_{an}/dt + R_0 \cdot i_{an} \tag{6.1b}$$

where u_{ap} and u_{an} are the total output voltages of the SMs in the upper and lower arms of phase *a*, respectively. From (6.1) and according to Kirchhoff's current law, v_a is obtained as follows

$$v_a = v_{a0} - L_0/2 \cdot di_a/dt - R_0/2 \cdot i_a \tag{6.2a}$$

$$v_{a0} = \left(V_{dc} - u_{ap} + u_{an}\right)/2 \tag{6.2b}$$

Based on (6.2), the equivalent circuit of a three-phase MMC for the load is depicted in Figure 6.2(a), where v_{b0} and v_{c0} are the corresponding voltages of phases *b* and *c* similarly defined as in (6.2b). In this paper, v_{h0} (*h*=*a*, *b*, or *c*) is called the "modulation voltage".

Meanwhile, the currents of the upper and lower arms of phase *a* are [27]

$$i_{ap} = i_{cir,a} + i_a/2 \tag{6.3a}$$

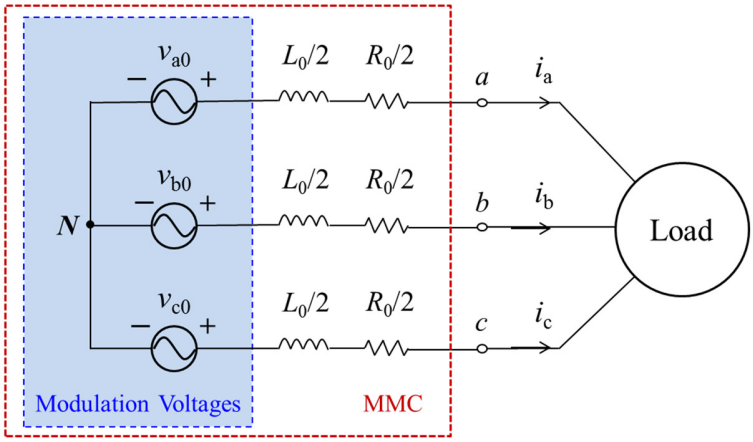
$$i_{an} = i_{cir,a} - i_a/2 \tag{6.3b}$$

where $i_{cir,a}=(i_{ap}+i_{an})/2$ is called the circulating current of phase *a* and is independent of the load. Based on Kirchhoff's voltage law, the circulating current is determined by [35]

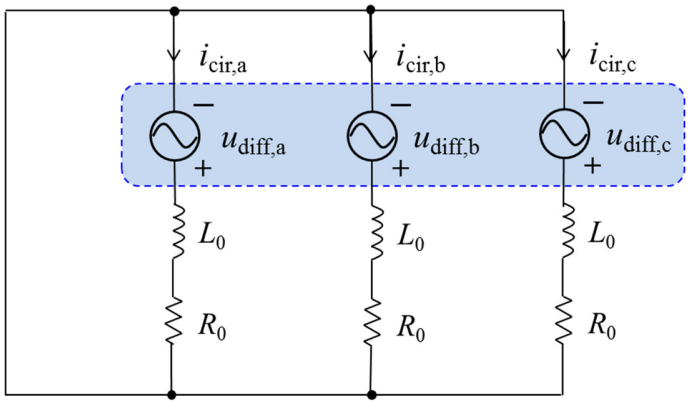
$$L_0 \cdot di_{cir,a}/dt + R_0 \cdot i_{cir,a} = u_{diff,a} = \left(V_{dc} - u_{ap} - u_{an}\right)/2 \tag{6.4}$$

where $u_{diff,a}$ is called the "difference voltage" of phase *a*. Accordingly, the equivalent circuit of the three-phase MMC for the circulating currents is shown in Figure 6.2(b), where $u_{diff,h}$ and $i_{cir,h}$ (*h*=*a*, *b*, or *c*) are respectively the difference voltage and circulating current of phase *h* similarly defined in (6.4).

Figure 6.2 reveals that the MMC can be controlled by regulating the modulation voltage v_{h0} (*h*=*a*, *b*, or *c*) and the difference voltage $u_{diff,h}$. The reference value of v_{h0} is determined in accordance with the load and the applications of the MMC, and can generally be obtained from a current regulator. On the other hand, the reference value of $u_{diff,h}$ is adjusted to control the circulating current and consequently the SM capacitor voltages, which will be introduced in detail later.



(a)



(b)

Figure 6.2 Equivalent circuit of a three-phase MMC: (a) for the load; (b) for the circulating currents.

When coupled buffer inductors are used, as shown in Figure 6.3, (6.1a) becomes

$$v_a = v_{a0} - (L_0 - M)/2 \cdot di_a/dt - R_0/2 \cdot i_a \tag{6.5}$$

where M is the mutual inductance. In this condition, the equivalent circuit shown in Figure 6.2(a) is still applicable, except that the series inductance is (L_0-M)/2 rather than L_0/2. Accordingly, (6.4) becomes

$$(L_0 + M) \cdot di_{cir,a}/dt + R_0 \cdot i_{cir,a} = u_{diff,a} \tag{6.6}$$

which means that the equivalent circuit shown in Figure 6.2(b) is also applicable, except that the inductance is L_0+M instead of L_0. The proof of (6.5) and (6.6) is presented in Appendix C.

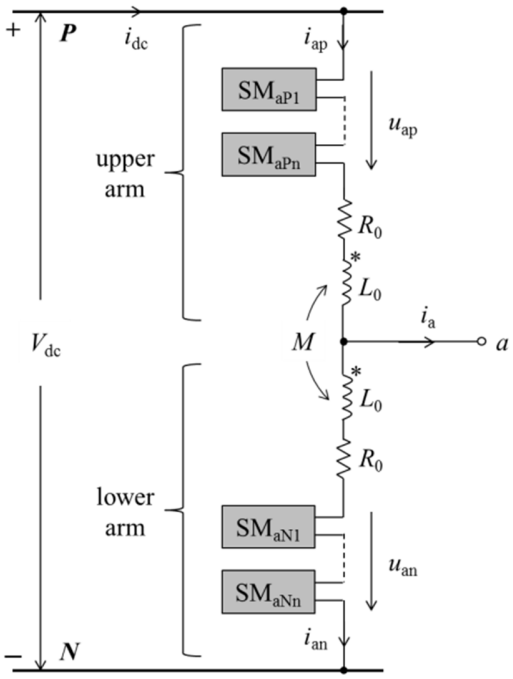


Figure 6.3 Circuit diagram (one phase) of an MMC when coupled buffer inductors are used.

6.1.2 Control of Capacitor Voltages and Circulating Currents

According to Figure 6.2, the energy stored in the capacitors of the upper arm (W_{ap}) and the lower arm (W_{an}) of phase *a* respectively deviate as follows

$$dW_{ap}/dt = u_{ap} \cdot i_{ap} \tag{6.7a}$$

$$dW_{an}/dt = u_{an} \cdot i_{an} \tag{6.7b}$$

By substituting (6.1)-(6.3) into the above equations, the derivatives of the total capacitor energy (W_{ap}+W_{an}) of phase *a* and the unbalanced energy (W_{ap}-W_{an}) between the upper and lower arms are obtained as

$$d(W_{ap} + W_{an})/dt = V_{dc} \cdot (i_{cir,a} + i_a/2) - 2u_{diff,a} \cdot i_{cir,a} - v_{a0} \cdot i_a \tag{6.8a}$$

$$d(W_{ap} - W_{an})/dt = V_{dc} \cdot (i_{cir,a} + i_a/2) - u_{diff,a} \cdot i_a - 2v_{a0} \cdot i_{cir,a} \tag{6.8b}$$

which show that the circulating current $i_{cir,a}$ plays a significant role for controlling the capacitor energies (i.e., the capacitor voltages in each arm).

More specifically, $i_{cir,a}$ and $u_{diff,a}$ can be expressed by their dc and harmonic components as follows

$$i_{cir,a} = I_{cir,a} + \sum_{k=1}^{\infty} i_{cir(k)} \tag{6.9a}$$

$$u_{diff,a} = U_{diff,a} + \sum_{k=1}^{\infty} u_{diff(k)} \tag{6.9b}$$

where $I_{\text{cir,a}}$ and $U_{\text{diff,a}}$ are the dc components, and $i_{\text{cir(k)}}$ and $u_{\text{diff(k)}}$ are the k^{th} order harmonics. Then, (6.8) is rewritten as

$$\frac{d(W_{ap}+W_{an})}{dt} = \underline{V_{dc} \cdot I_{cir,a} - 2u_{diff,a} \cdot i_{cir,a} - v_{a0} \cdot i_a} + V_{dc} \cdot \left(\sum_{k=1}^{\infty} i_{cir(k)} + \frac{i_a}{2}\right) \tag{6.10a}$$

$$\begin{aligned}\frac{d(W_{ap}-W_{an})}{dt} = {} & \underline{V_{dc} \cdot I_{cir,a} - u_{diff(1)} \cdot i_a - 2v_{a0} \cdot \left(I_{cir,a} + i_{cir(1)}\right)} \\ & + V_{dc} \cdot \left(\sum_{k=1}^{\infty} i_{cir(k)} + \frac{i_a}{2}\right) - \left(U_{diff,a} + \sum_{k=2}^{\infty} u_{diff(k)}\right) \cdot i_a - 2v_{a0} \cdot \sum_{k=2}^{\infty} i_{cir(k)}\end{aligned} \tag{6.10b}$$

where only the parts highlighted by underlines contribute to dc components (v_{a0} is assumed to contain only dc and fundamental frequency components). The dc components should be zero in the steady state; otherwise, the total capacitor energy or unbalanced energy will increase or decrease continuously.

It is demonstrated by (6.10a) that the dc component of the circulating current can be regulated to maintain the total capacitor energy. The active power provided by the dc-link voltage then is delivered to the load and compensates for the power losses of the phase leg. On the other hand, (6.10b) indicates that the unbalanced capacitor energy between the upper and lower arms can be controlled by regulating the fundamental frequency component of the difference voltage $u_{\text{diff,a}}$ that is in phase with the output current i_{a}, or the fundamental frequency component of the circulating current that is in phase with (the fundamental frequency component of) the modulation voltage v_{a0}. Similar conclusions can be obtained for the other phases.

Figure 6.4 shows a control diagram for capacitor voltages and circulating currents, taking phase *a* as an example. It consists of three control loops, i.e., the averaging control, the circulating current control, and the arm-balancing control; and finally a reference value $u_{\text{diff,a}}^{*}$ of the difference voltage is generated. Corresponding to (6.10a), the

averaging control forces the average capacitor voltage $\overline{v}_{C,a}$ of the phase to follow its reference value v_C^*, with

$$\overline{v}_{C,a} = (\overline{v}_{C,ap} + \overline{v}_{C,an})/2 \tag{6.11a}$$

$$\overline{v}_{C,ap} = (\sum_{i=1}^{n} v_{C,api})/n \tag{6.11b}$$

$$\overline{v}_{C,an} = (\sum_{i=1}^{n} v_{C,ani})/n \tag{6.11c}$$

where $\overline{v}_{C,ap}$ and $\overline{v}_{C,an}$ are the average capacitor voltages of the upper and lower arms of phase a, respectively; $v_{C,api}$ is the capacitor voltage of the i^{th} SM in the upper arm; and $v_{C,ani}$ is the capacitor voltage of the i^{th} SM in the lower arm. The averaging control gives a reference value $I_{cir,a}^*$ of the dc component of the circulating current. Based on (6.10b), the arm-balancing control loop generates a fundamental frequency component $u_{diff(1)}^*$ of the difference voltage, to cancel the capacitor voltage difference between the upper and lower arms.

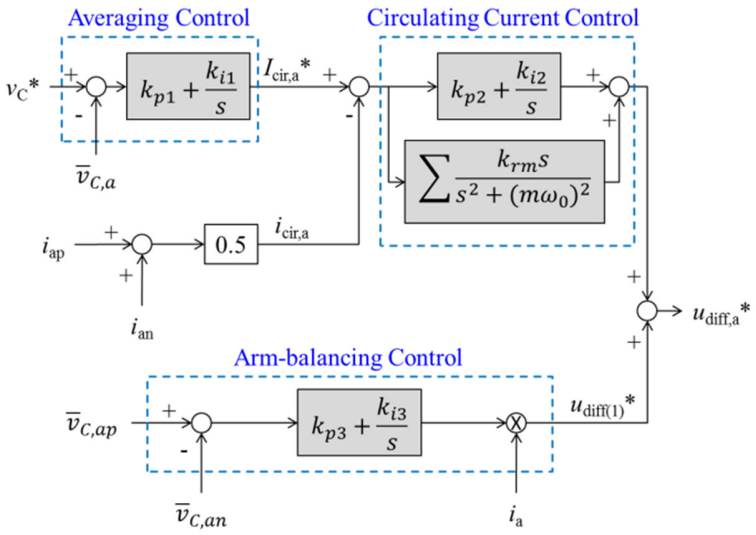


Figure 6.4 Control of the capacitor voltages and circulating current for one phase (phase *a* as an example).

The circulating current control loop forces the circulating current to follow the reference dc component $I_{cir,a}^*$, as well as eliminates second-order (and higher-order if

needed) components of the circulating current. Similar to the averaging control and arm-balancing control, the circulating current control loop applies a proportional-integral (PI) controller to track the reference dc component. A set of resonant controllers [81] expressed as follows

$$G_r(s) = \sum \frac{k_{rm} s}{s^2 + (m\omega_0)^2} \tag{6.12}$$

where ω_0 is the fundamental angular frequency and k_{rm} is the coefficient for the m^{th} order resonant frequency, is utilized to eliminate the corresponding harmonics.

According to (6.4), the circulating current control loop in fact regulates the dc and second-order (and higher-order if the corresponding resonant controller is applied) components of the difference voltage. Finally, a reference value $u_{diff,a}^*$ of the difference voltage is generated to achieve the capacitor voltage and circulating current control.

Figure 6.5 shows the closed-loop diagram of the circulating current control, taking (6.4) into account. The open-loop transfer function is:

$$G_o(s) = \left(k_{p2} + \frac{k_{i2}}{s} + \sum \frac{k_{rm} s}{s^2 + (m\omega_0)^2}\right) \cdot \frac{1}{sL_0 + R_0} \tag{6.13}$$

At the resonant frequency $m\omega_0$, the gain of $G_o(s)$ is infinite, so the m^{th} order harmonic of the circulating current is eliminated in the steady state. More detailed analysis of the circulating current control is presented in Appendix C.

Note that the control of capacitor voltages and circulating currents may also be implemented in other approaches. For example, it can be designed to force the circulating current to contain only the dc component [73] [81], which minimizes the power losses of the MMC but may increase the ripples of the capacitor voltages according to (6.10). Injecting specific circulating currents based on the steady state or instantaneous information of the MMC to reduce the capacitor voltage ripples is investigated in [77]. Based on the synchronous reference frame, PI controllers instead of resonant controllers can be adopted to eliminate specific harmonics of the circulating currents [28]. However, it is a common point of those methods that the control of capacitor voltages and

circulating currents is achieved by regulating the reference difference voltage $u_{\text{diff,h}}^*$ (h=a, b, or c) for each phase of the MMC.

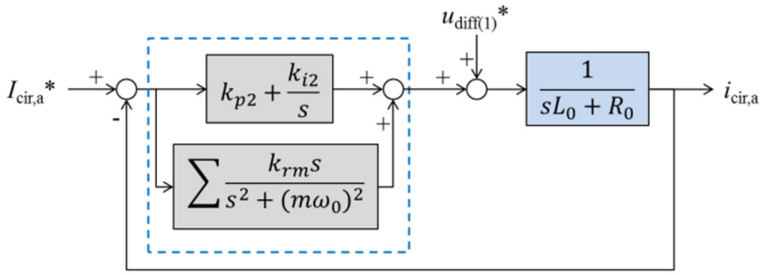


Figure 6.5 Closed-loop diagram of the circulating current control.

6.2 Proposed SVM Method for the MMC

6.2.1 Generating the Modulation Voltages for the Load

The general multilevel SVM scheme introduced in Chapter 4 [97], as illustrated in Figure 6.6 based on the space vector diagram of a five-level converter, is briefly reviewed in this section and is applied to generate the reference value v_{h0}^* (h=a, b, or c) of the modulation voltage v_{h0} required by the load. Accordingly, the reference vector $\boldsymbol{V}_{\text{ref}}$ is obtained [38] [44] [97] as follows

$$\boldsymbol{V}_{ref} = (N-1)\left(v_{a0}^* + v_{b0}^* \cdot e^{j\frac{2}{3}\pi} + v_{c0}^* \cdot e^{j\frac{4}{3}\pi}\right) = (N-1)\left(M \cdot \frac{\sqrt{3}}{2} V_{dc} \cdot e^{j\theta}\right) \tag{6.14}$$

where N is the number of voltage levels; M ($= \hat{v}_{ab}/V_{dc}$) is the modulation index, where $\hat{v}_{ab}$ is the peak value of the reference line-to-line voltage ($v_{a0}^* - v_{b0}^*$); and θ is the phase angle of $\boldsymbol{V}_{\text{ref}}$.

A candidate switching state $S_aS_bS_c$, for the vertex (i.e., P_2) of the modulation triangle $\Delta P_1P_2P_3$ (i.e., the nearest three vectors $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$) closest to the origin, is detected by the general SVM in a single step [97]:

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \min(x, y, -y) \\ y - \min(x, y, -y) \\ -y - \min(x, y, -y) \end{bmatrix}\right) \tag{6.15}$$

where min(x, y, $-y$) denotes the minimum value among x, y, and $-y$; int(γ) stands for the corresponding integer parts of all the elements in an array γ; and

$$x = \frac{V_{ref(x)}}{V_{dc}}, \quad y = \frac{V_{ref(y)}}{\sqrt{3}V_{dc}} \tag{6.16}$$

where $V_{\mathrm{ref(x)}}$ and $V_{\mathrm{ref(y)}}$ are respectively the real and imaginary components of the reference vector.

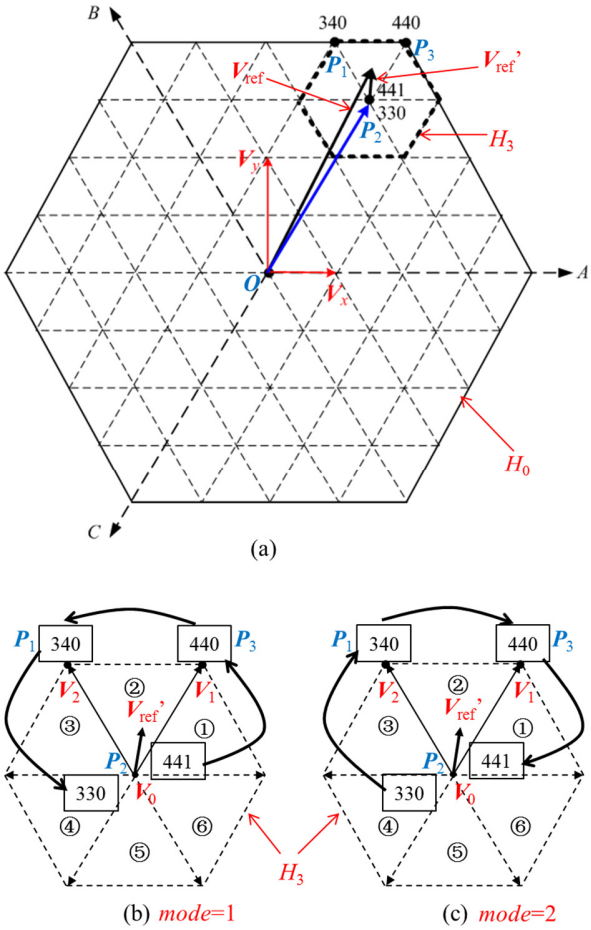


Figure 6.6 General SVM scheme in Chapter 4 [97]: (a) detecting the modulation triangle; (b)-(c) two switching sequence modes.

Based on a so-called "remainder vector" $\boldsymbol{V}_{\mathrm{ref}}$' shown in Figure 6.6(b) and (c), which is yielded by shifting the origin of the reference vector $\boldsymbol{V}_{\mathrm{ref}}$ to the detected vertex (P_2), the duty cycles of the nearest three vectors are determined in the same way as for a two-level SVM [97]:

$$\begin{cases} d_1 = \frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg}{3}\pi\right) - V_{ry}\cos\left(\frac{reg}{3}\pi\right)\right] \\ d_2 = -\frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg-1}{3}\pi\right) - V_{ry}\cos\left(\frac{reg-1}{3}\pi\right)\right] \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{6.17}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{ref}'/V_{dc}$, respectively; d_1 and d_2 are respectively the duty cycles of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$; d_0 is the total duty cycle for the "zero vectors", i.e., the switching states at the detected vertex (e.g., 441 and 330 at P_2); *reg* is the region number (①-⑥) of the remainder vector $\boldsymbol{V}_{ref}'$ in the two-level hexagon H_3 and is given [97] by

$$reg = \text{int}(3\theta_{rem}/\pi) + 1 \tag{6.18}$$

where θ_{rem} ($0 \le \theta_{rem} < 2\pi$) is the angle of the remainder vector with respect to the real axis, and int($3\theta_{rem}/\pi$) represents the integer part of $3\theta_{rem}/\pi$. In this chapter, each switching sequence (e.g., 441 → 440 → 340 → 330) contains two zero vectors, and the duty cycles d_{01} and d_{02} of the two zero vectors are set to be equal (i.e., d_{01}=d_{02}=0.5d_0) for the objective of the optimal harmonic performance [58].

It has been demonstrated in [38] [97] that any optimized switching sequences (with the minimum number of switch transitions in every switching cycle) can be equivalently achieved by two successive switch states K_h and K_h+1 for phase *h* (*h*=*a*, *b*, or *c*), as long as the duty cycles of K_h and K_h+1 (i.e., 1-D_h and D_h, respectively) are the values summarized in Table 4.2. In addition, $K_aK_bK_c$ and (K_a+1)(K_b+1)(K_c+1) are the two "zero vectors".

The switching state $K_aK_bK_c$ is a redundant switching state for the detected vertex (P_2), so it can be generated [97] based on (6.15) as follows

$$\begin{bmatrix} K_a \\ K_b \\ K_c \end{bmatrix} = \begin{bmatrix} S_a + N_0 \\ S_b + N_0 \\ S_c + N_0 \end{bmatrix}, \quad \text{where the integer } N_0 \in [0,\ N - 2 - \max(S_a, S_b, S_c)] \tag{6.19}$$

where max(S_a, S_b, S_c) is the maximum value among S_a, S_b, and S_c. The maximum value of N_0 is N-2-max(S_a, S_b, S_c) because otherwise K_h+1 (*h*=*a*, *b*, or *c*) exceeds N-1. Compared

with other modulation methods, the SVM scheme provides the significant flexibility to optimize the performance of the MMC by selecting the optimal N_0.

With the switching state K_h and duty cycle D_h for phase h (h=a, b, or c), the actual modulation voltage applied to phase h of the MMC is [38]

$$v_{h0} = (1 - D_h) \cdot \frac{K_h V_{dc}}{N-1} + D_h \cdot \frac{(K_h+1)V_{dc}}{N-1} = (K_h + D_h)V_{dc}/(N-1) \tag{6.20}$$

Assume that k_{hp} and k_{hn} ($0 \leq k_{hp}, k_{hn} \leq n$) SMs respectively in the upper and lower arms of phase h are in the "ON" state. If the capacitor voltages are assumed to be well balanced, i.e., $v_C = V_{dc}/n$ for any SM, then (6.2b) is rewritten as

$$v_{h0} = \left(V_{dc} - k_{hp} \cdot V_{dc}/n + k_{hn} \cdot V_{dc}/n\right)/2 \tag{6.21}$$

Combining (6.20) and (6.21) yields the following relationship:

$$n - k_{hp}^* + k_{hn}^* = 2n \cdot (K_h + D_h)/(N-1) \tag{6.22}$$

where * represents the reference value. Since (6.22) offers some flexibility of selecting k_{hp} and k_{hn}, this flexibility is used to control the circulating currents and capacitor voltages, as introduced later.

Note that as shown in (6.21), $0 \leq v_{h0} \leq V_{dc}$ and the minimum voltage step for v_{h0} is $V_{dc}/(2n)$, so theoretically the maximum level number is $N = 2n+1$. In other words, because of the equivalent circuit in Figure 6.2, the proposed SVM method naturally generates the maximum number of levels.

6.2.2 Applying the Reference Difference Voltage

In order to control the capacitor voltages and circulating currents, the reference difference voltage $u_{diff,h}^*$ obtained from Figure 6.4 for phase h (h=a, b, or c) needs to be applied. Combining (6.4) and (6.22) then gives reference values for k_{hp} and k_{hn} as follows

$$k_{hp}^* = n - \frac{n}{N-1} \cdot (K_h + D_h) - \frac{n}{V_{dc}} \cdot u_{diff,h}^* \tag{6.23a}$$

$$k_{hn}^* = \frac{n}{N-1} \cdot (K_h + D_h) - \frac{n}{V_{dc}} \cdot u_{diff,h}^* \tag{6.23b}$$

Finally, a general solution for each k_{hi} (i=p or n) during a switching cycle T_s is obtained as:

1) If $k_{hi}^* \leq 0$,

$$k_{hi} = 0 \tag{6.24a}$$

2) If $k_{hi}^* \geq n$,

$$k_{hi} = n \tag{6.24b}$$

3) If $0 < k_{hi}^* < n$,

$$k_{hi} = \begin{cases} \text{int}(k_{hi}^*), & \text{when } 0 < t \leq (1-\alpha)T_s \\ \text{int}(k_{hi}^*) + 1, & \text{when } (1-\alpha)T_s < t \leq T_s \end{cases} \tag{6.24c}$$

where int(k_{hi}^*) represents the integer part of k_{hi}^*, and

$$\alpha = k_{hi}^* - \text{int}(k_{hi}^*) \tag{6.25}$$

Figure 6.7 illustrates the way to generate k_{hi} (h=a, b, or c; i=p or n) for each arm of the MMC during a switching cycle T_s, where *cr* is a carrier wave. The implementation of the proposed SVM method is as easy as the nearest-level modulation method [34]-[37].

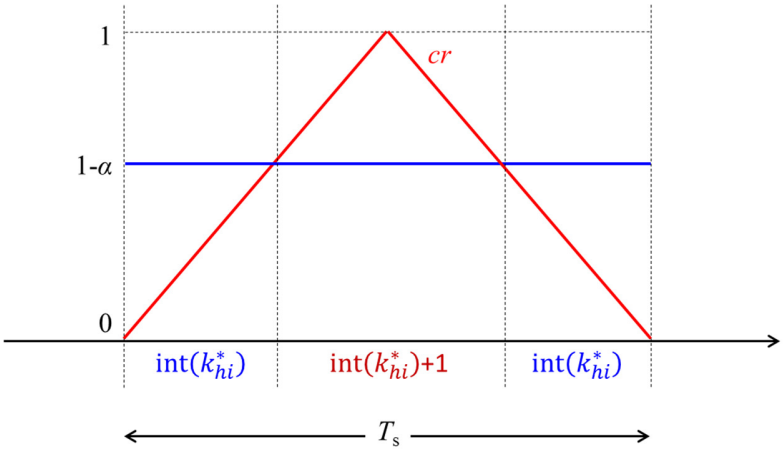


Figure 6.7 Generation of k_{hi} (h=a, b, or c; i=p or n) during a switching cycle T_s.

6.2.3 Optimized Control Strategy

For each redundant switching state $K_aK_bK_c$ generated in (6.19) by the SVM scheme, the number of ON-state SMs for each arm of the MMC is given by (6.24). The MMC

usually consists of a large number of SMs, so the number of redundant switching states is usually large, especially for small modulation indices [38] [44] [97]. This offers significant flexibility for optimizing the control performance. The objective is to find the optimal redundant switching state, i.e., the optimal N_0 in (6.19).

Assume the total capacitor voltages in the upper and lower arms of phase h (h=a, b, or c) at a sampling instant t_0 are respectively $v_{C,hp}$ and $v_{C,hn}$. According to (6.24), after a switching cycle T_s, $v_{C,hi}$ (i=p or n) then becomes

$$v'_{C,hi} = v_{C,hi} + \frac{i_{hi}}{C}\int_{t_0}^{t_0+T_s} k_{hi}dt = \begin{cases} v_{C,hi}, & \text{if } (k^*_{hi} \le 0); \\ v_{C,hi} + \frac{n \cdot i_{hi} \cdot T_s}{C}, & \text{if } (k^*_{hi} \ge n); \\ v_{C,hi} + \frac{k^*_{hi} \cdot i_{hi} \cdot T_s}{C}, & \text{if } (0 < k^*_{hi} < n). \end{cases} \tag{6.26}$$

where C is the capacitance of the SM capacitors.

To achieve the best capacitor voltage balancing, the optimal N_0 should minimize the following objective function

$$J = \sum_{h=a,b,c}\left\{\left(v'_{C,hp} - V_{dc}\right)^2 + \left(v'_{C,hn} - V_{dc}\right)^2\right\} \tag{6.27}$$

The optimal N_0 (named N_{0_opt}) is therefore found by computing and comparing J for all the possible values of N_0, as shown in Figure 6.8. Optimized SM capacitor voltages also lead to improved circulating currents since they are mutually coupled.

Note that this paper only optimizes the selection of redundant switching states, for purposes of the optimal harmonic performance and simple implementation. If needed, the duty cycles d_{01} and d_{02} of the zero vectors can also be optimized to further improve the control performance [75].

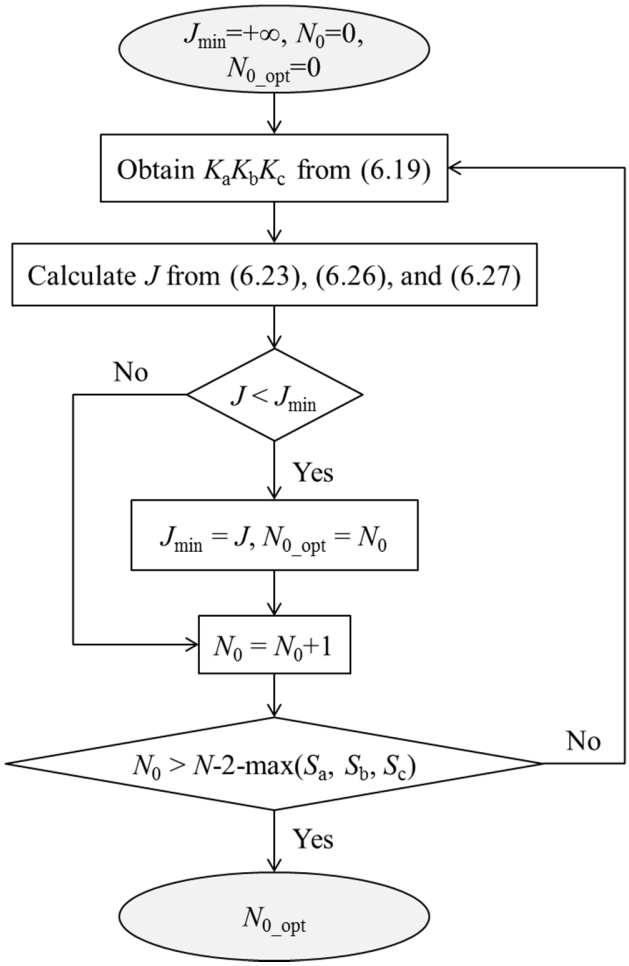


Figure 6.8 Determination of N_{0_opt} (the optimal N_0).

6.2.4 Selection of SMs

After k_{hp} and k_{hn} of phase h (h=a, b, or c) are obtained from (6.24), the capacitor voltages of the SMs in each arm are balanced by selecting the appropriate ON-state SMs according to the direction of the arm current, known as the so-called "sorting method" [32] [36]. The basic principles are as follows:

1) If the arm current is positive, the SMs with the lowest capacitor voltages are selected to be the ON-state, so that the capacitors of these SMs are charged.

2) If the arm current is negative, the SMs with the highest capacitor voltages are selected to be the ON-state, so that the capacitors of these SMs are discharged.

6.2.5 Summary

Figure 6.9 illustrates the diagram of the proposed SVM method, which represents a general framework for implementing SVM-based control for the MMC. It can be conveniently extended for other control objectives, by replacing the capacitor voltage and circulating current control block with customized controllers.

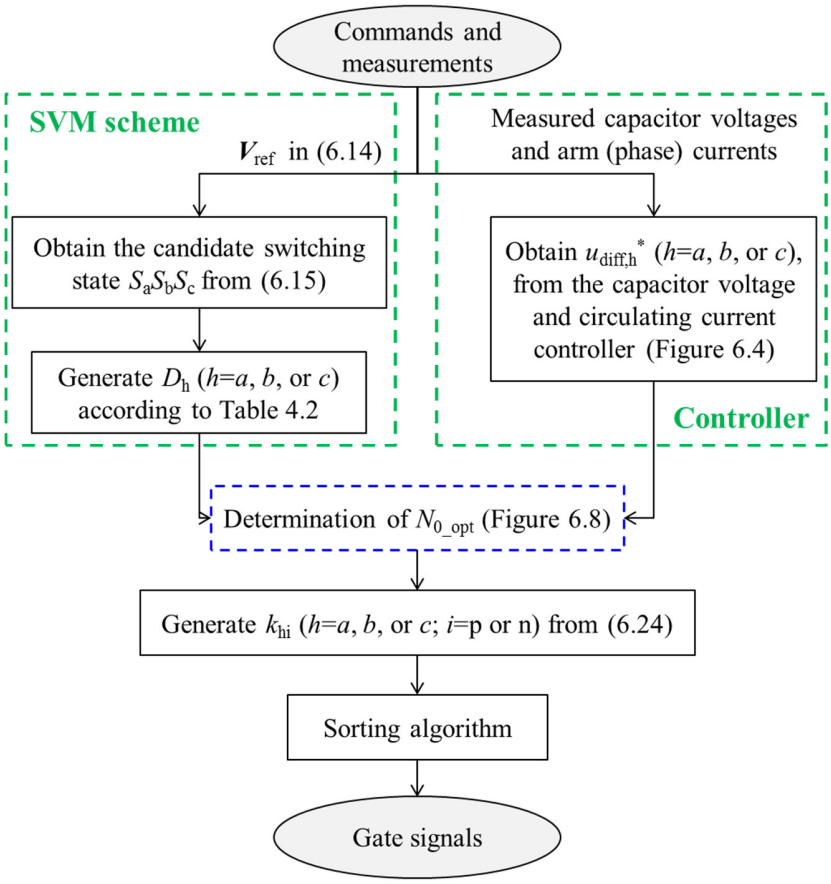


Figure 6.9 The proposed SVM method for the MMC.

6.3 Simulation Results

Simulations are carried out to demonstrate the proposed SVM method, based on a three-phase MMC with the parameters shown in Table 6.1. The control parameters (capacitor voltages are divided by the reference value before being sent to the controller) in Figure 6.4 are presented in Table 6.2.

Table 6.1 Parameters of the MMC for Simulation

Parameter	Value
DC-link voltage (V_{dc})	400 V
No. of SMs per arm (n)	4
SM capacitor reference voltage (v_C^*)	100 V
SM capacitance (C)	1.41 mF
Arm inductance (L_0)	2.2 mH
Parasitic resistor in each arm (R_0)	88.88 mΩ
Carrier frequency (f_s)	5 kHz
Modulation index (M)	0.9 or 0.5
Voltage level number (N)	9
Load resistance (R_L) and inductance (L_L) per phase (Y-connected)	15 Ω + 37.5 mH
Fundamental frequency (f_0)	50 Hz
Simulation time step (Δt)	20 μs

Table 6.2 Control Parameters

Controller	Parameters
Averaging control	k_{p1}=10, k_{i1}=120
Circulating current control	k_{p2}=10, k_{i1}=200; k_{r2}=400; k_{r4}=300
Arm-balancing control	k_{p3}=30, k_{i3}=500

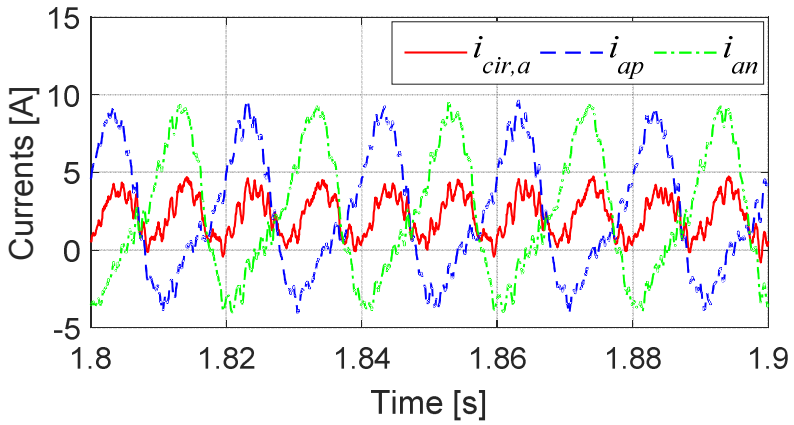
For the sake of fair comparisons, the optimization of redundant switching states is not activated, and

$$N_0 = \text{round}\left(\frac{N-2-\max(S_a,S_b,S_c)}{2}\right) \tag{6.28}$$

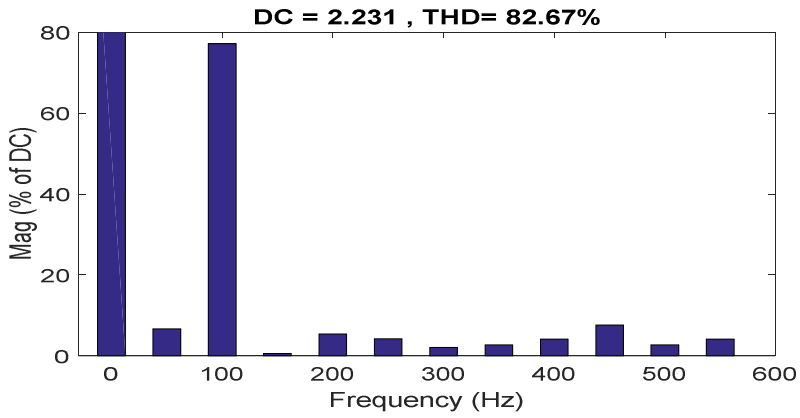
is adopted in this section, where round(x) represents the nearest integer of x. The modulation index M is 0.9 unless otherwise specified, in order to display all the voltage levels.

6.3.1 Performance of the Circulating Current Controller

Figure 6.10(a) shows the simulated arm and circulating currents of phase a, when the circulating current control in Figure 6.4 only applies the PI controller (i.e., the resonant controllers are unused). The harmonic spectrum of the circulating current appears in Figure 6.10(b). It is observed that without the resonant controllers, the circulating current contains abundant harmonics, especially the 2nd order harmonic component.



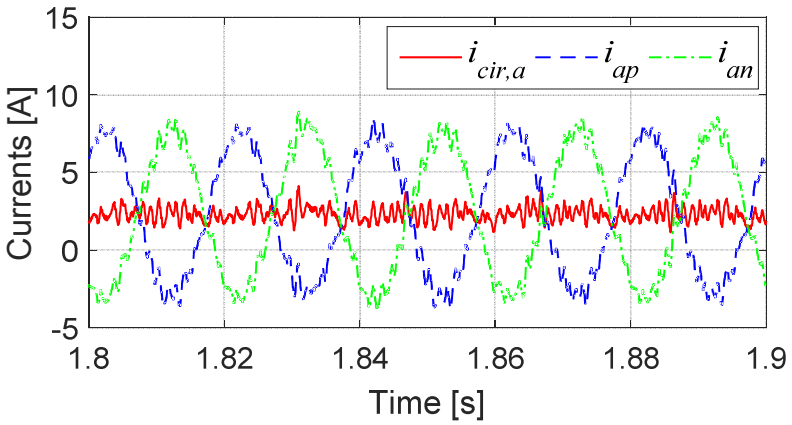
(a)



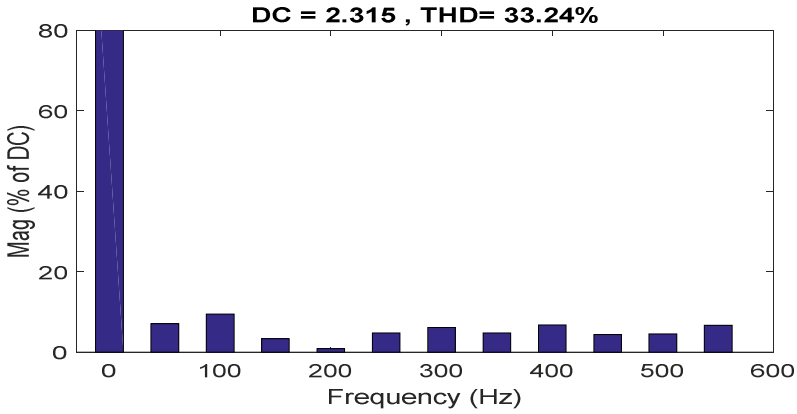
(b)

Figure 6.10 Simulation results when the circulating current control only applies the PI controller: (a) arm and circulating currents of phase *a*; (b) harmonic spectrum of the circulating current.

Theoretically, more resonant controllers lead to a better performance of the circulating current suppression, but increase the computational burden. This paper uses two resonant controllers (k_{r2}=400 and k_{r4}=300) for demonstration purposes. When the resonant controllers are added, Figure 6.11 shows the simulated arm and circulating currents of phase *a*, as well as the harmonic spectrum of the circulating current. Comparison with Figure 6.10 demonstrates that the 2nd (100 Hz) and 4th (200 Hz) order harmonics of the circulating current are significantly suppressed.



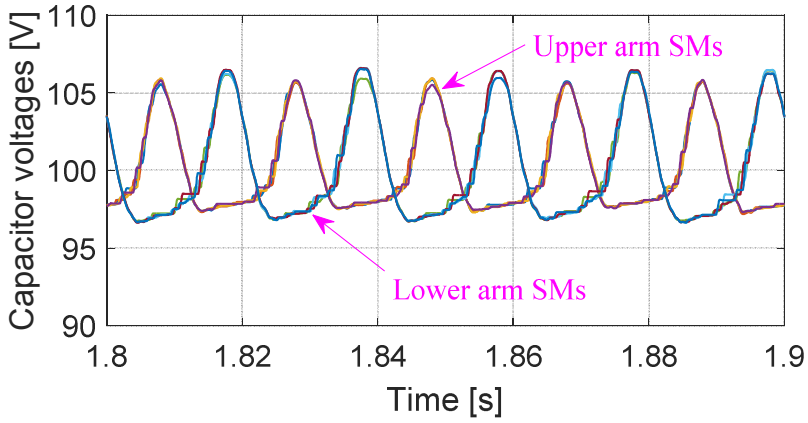
(a)



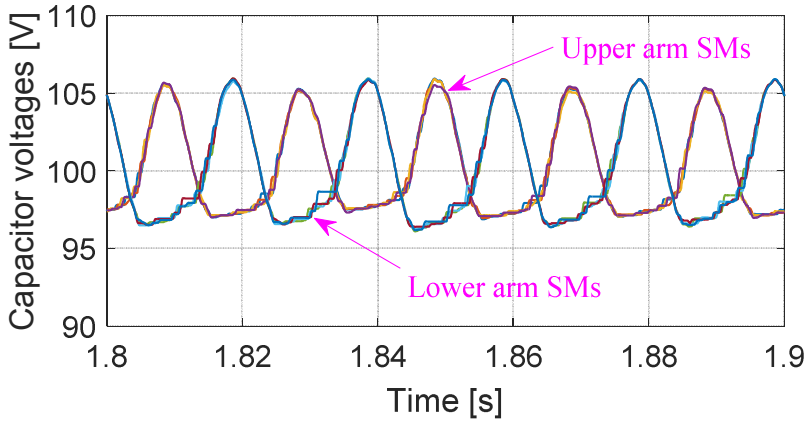
(b)

Figure 6.11 Simulation results when the resonant controllers are added to the circulating current control: (a) arm and circulating currents of phase *a*; (b) harmonic spectrum of the circulating current.

Figure 6.12 illustrates the simulated SM capacitor voltages of phase *a*, with and without the resonant controllers. The SM capacitor voltages are all regulated to the reference value. Therefore, eliminating the (2^{nd} and higher order) harmonics of the circulating current reduces the power losses of the MMC while not harming the capacitor voltage balancing. In fact, reduced harmonics of the circulating current also lead to an improved capacitor voltage balancing control since the SM capacitor voltages are mutually coupled with the circulating current, though the improvement is slight for this simulation condition.



(a)



(b)

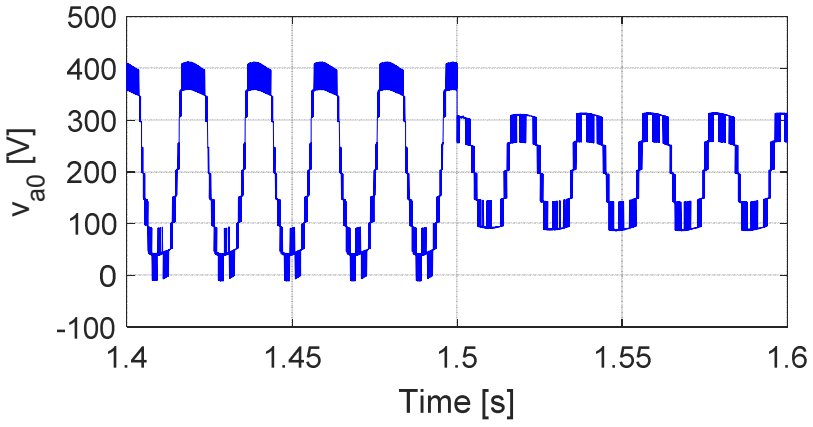
Figure 6.12 Simulated SM capacitor voltages of phase *a* using different circulating current controllers: (a) PI; (b) PI and resonant controllers.

6.3.2 Maximum Voltage Level Number

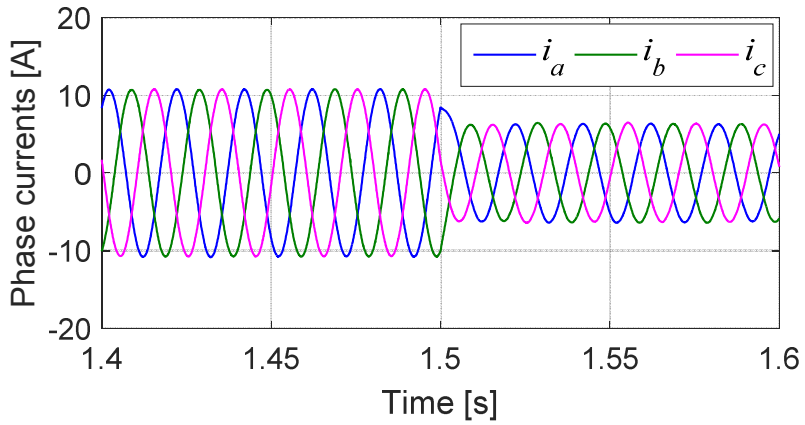
Figure 6.13 presents the simulated modulation voltage v_{a0} and phase currents for different modulation indices. When the time t<1.5 s, M=0.9; M changes to 0.5 at t=1.5 s. It is observed in Figure 6.13(a) that the maximum voltage level number (N=9) is achieved for v_{a0}.

For a low modulation index (e.g., M=0.5), not all the available voltage levels are utilized if the redundant switching states are not optimally selected, as in (6.28). Therefore, considerable flexibility is lost without optimizing the redundant switching

states. Section 6.4 experimentally demonstrates the advantages when the optimized control strategy in Figure 6.8 is applied.



(a)



(b)

Figure 6.13 Simulation results for different modulation indices (M changes from 0.9 to 0.5 at 1.5 s): (a) modulation voltage v_{a0}; (b) phase currents.

6.4 Experimental Results

The proposed SVM method is also tested based on the experimental setup of a three-phase MMC shown in Figure 6.14, according to the operating conditions summarized in Table 6.3 and the control parameters presented in Table 6.2. A DC power supply maintains a 160 V dc-link voltage for the MMC. A real-time simulator OPAL-RT [99] is used to implement the proposed SVM method in real time and to generate the gate signals for the MMC's power switches. The OPAL-RT interfaces (receives commands

and sends real-time results) with a command station (laptop) via TCP/IP protocol. For the experimental results presented later, the SM capacitor voltages directly use the data sampled by the OPAL-RT from the voltages sensors, while the other measured results are recorded through an oscilloscope.

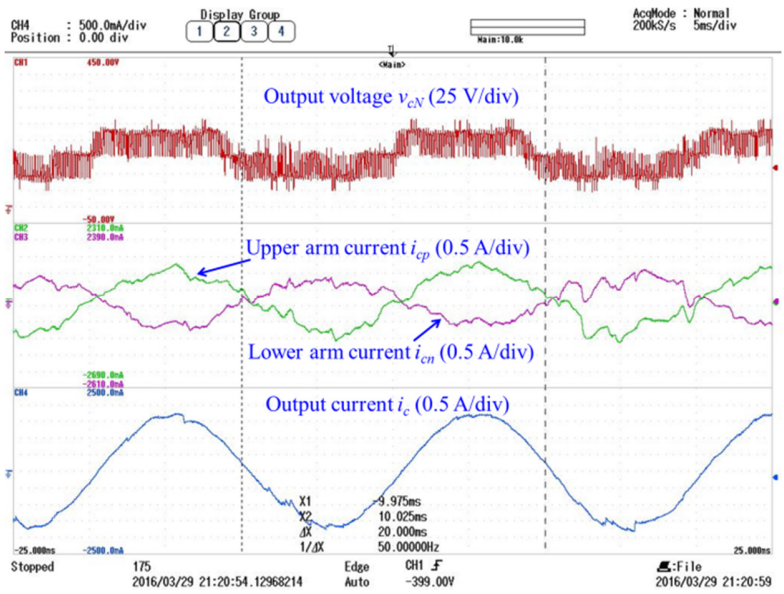
Figure 6.14 Experimental setup.

Table 6.3 Parameters of the Experimental Setup

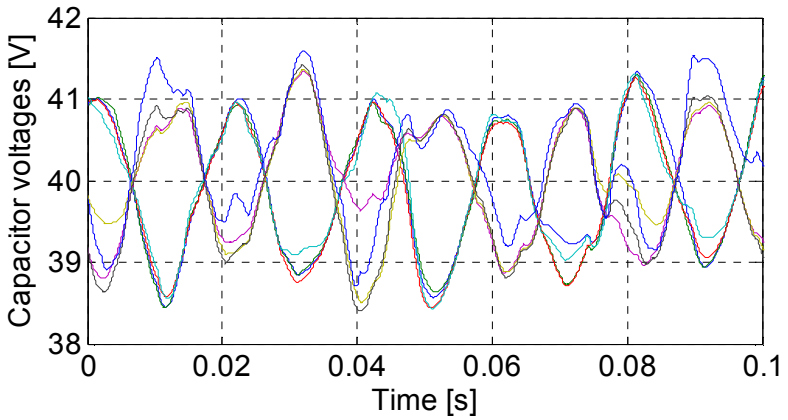
Parameter	Value
DC-link voltage (V_{dc})	160 V
No. of SMs per arm (n)	4
SM capacitor reference voltage (v_C^*)	40 V
SM capacitance (C)	1.41 mF
Arm inductance (L_0)	10 mH
Parasitic resistor in each arm (R_0)	88.88 mΩ
Carrier frequency (f_s)	5 kHz
Modulation index (M)	0.4
Voltage level number (N)	9
Load resistance (R_L) and inductance (L_L) per phase (Y-connected)	15 Ω + 10 mH
Fundamental frequency (f_0)	50 Hz
OPAL-RT time step (Δt)	20 μs

Figure 6.15 shows the measured output voltage, arm currents, output current, and SM capacitor voltages of one phase (e.g., phase c), when the optimization of redundant

switching states is not activated and (6.28) is adopted. As previously explained, the output voltage does not utilize all the available voltage levels, for the low modulation index (M=0.4) test condition. The maximum ripple (peak-to-peak) of the SM capacitor voltages reaches 3 V (7.5% of the reference capacitor voltage).



(a)

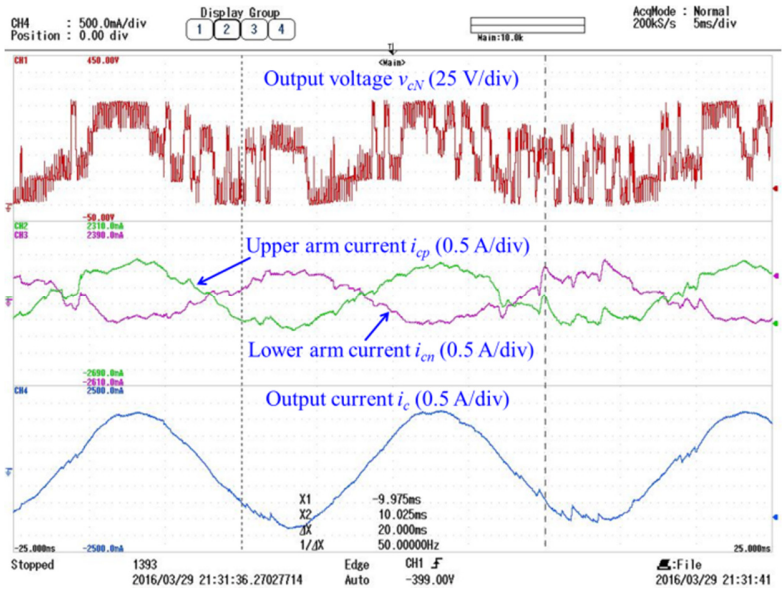


(b)

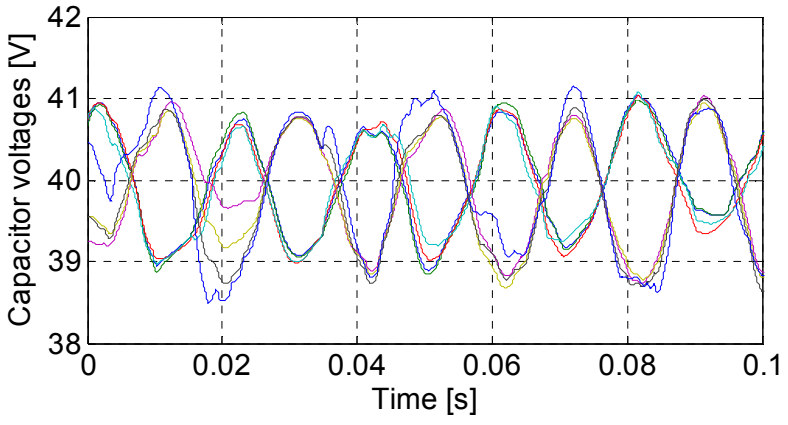
Figure 6.15 Experimental results when the optimized control strategy is not applied: (a) output voltage, arm currents, and output current of phase c; (b) SM capacitor voltages of phase c.

The corresponding experimental results, when the optimized control strategy in Figure 6.8 is applied, are shown in Figure 6.16. Significantly different from the voltage

waveform in Figure 6.15(a), now the output voltage contains all the available voltage levels. The output voltage no longer repeats every fundamental cycle because the optimal redundant switching state (optimal N_0) is adjusted every switching cycle according to the measured SM capacitor voltages and arm currents. Because of the optimized control strategy, the maximum ripple of the SM capacitor voltages is reduced to 2.5 V (i.e., 1/6 of the original maximum ripple is further reduced).



(a)



(b)

Figure 6.16 Experimental results based on the optimized control strategy: (a) output voltage, arm currents, and output current of phase *c*; (b) SM capacitor voltages of phase *c*.

6.5 Chapter Summary

This chapter has proposed a general SVM method for the MMC. An optimized control strategy for capacitor voltage balancing and circulating current suppression has been presented as well, by utilizing the redundant switching states offered by the SVM scheme. Compared with earlier modulation methods for the MMC, this proposed new SVM method generates the maximum level number (i.e., $2n+1$, where n is the number of SMs in the upper or lower arm of each phase) of the output phase voltages, based on a new equivalent circuit of the MMC. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed new method is well suited to the MMC with a large number of SMs. Simulation and experimental results, for a three-phase MMC with four SMs in each arm, verify the proposed new method.

The next chapter summarizes the conclusions and contributions of this dissertation work and recommendations for future investigations.

CHAPTER 7 CONCLUSIONS, CONTRIBUTIONS, AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusions

Wind energy generation has grown rapidly around the world, resulting mostly from increasing concerns about energy security and sustainability. Variable-speed wind energy conversion systems, based on power electronic converters, are commonly adopted in modern wind energy plants to maximize capturing energy from the wind. To deliver the wind energy more efficiently and cost-effectively, high voltage direct current (HVDC) systems based on power electronic converters have attracted much attention. The increasing sizes of wind turbines and wind farms challenge the power electronic converters, and multilevel converters are therefore required to overcome the voltage and current limits of the power semiconductors. The proposed research focuses on developing modulation and control methods for multilevel converters so as to optimize their applications in wind energy generation and transmission.

Among various pulse width modulation (PWM) methods for multilevel converters, space vector modulation (SVM) provides more flexibility (i.e., redundant switching sequences and adjustable duty cycles) to optimize switching waveforms, but requires more complicated implementation because it simultaneously deals with all phases. This dissertation first investigates the inherent relationship between the SVM and a phase-voltage modulation technique, called the nearest-level modulation. It is demonstrated that the two modulation methods are functionally equivalent: with proper common-mode voltage injections, the nearest-level modulation method is equivalent to the SVM method; by selecting the appropriate redundant switching sequences and the corresponding duty cycles, the SVM method is equivalent to the nearest-level modulation method.

Consequently, a simplified SVM scheme for multilevel converters is proposed, which is independent of the level number of the converter and for the first time achieves the same easy implementation as phase-voltage modulation techniques. Compared with earlier SVM methods, the proposed scheme significantly simplifies the detection of the nearest three vectors and the generation of switching sequences (by avoiding lookup tables for switching states/sequences). A comparison of computational efficiency demonstrates that the proposed scheme requires the shortest computation time ($0.0467*10^{-3}$ s), even when the fastest earlier method ($0.0513*10^{-3}$ s) is further improved by using the rule of generating switching sequences introduced in this dissertation. Based on two orthogonal unit-vectors that decouple the components of different phases, the proposed scheme can potentially be extended to multiphase multilevel applications.

The three-level active neutral-point-clamped (ANPC) converter is well suited to control high-power wind turbine generators (typically below 6.6 kV and 10 MW), but suffers from unequal power loss distribution among its semiconductor devices. This dissertation proposes a new modulation scheme, called the *adaptive doubled frequency* PWM (ADF-PWM) scheme, to achieve the power loss balancing control for the ANPC converter. It possesses the same advantage as an earlier modulation scheme called the DF-PWM (doubled frequency PWM) scheme, i.e., a doubled apparent switching frequency (the equivalent switching frequency observed from the output voltage waveforms), but the new scheme offers a significantly improved power loss distribution and thermal dynamic. The basic idea of the proposed scheme is to adaptively adjust the duty cycles of the switching states for every switching cycle, in order to optimize the power loss distribution. Compared to the DF-PWM, in the experimental example the ADF-PWM further reduces the junction temperature of the most stressed semiconductor device from 80.6 ºC to 77.7 ºC, at no additional cost.

This dissertation also investigates the influence of the fundamental frequency on the thermal dynamics of the ANPC converter. It demonstrates that low fundamental

frequencies further aggravate the converters' power loss and junction temperature unbalance. Since the proposed ADF-PWM scheme optimizes the power loss distribution for every switching cycle, both average and instantaneous/peak junction temperatures of the most stressed semiconductors are reduced by the ADF-PWM scheme, especially at low fundamental frequencies. The simulation example shows that compared with the DF-PWM scheme, the ADF-PWM scheme further reduces the peak junction temperature of the most stressed semiconductor device by 3.0 ºC at 50 Hz (from 130.9 ºC to 127.9 ºC) and 5.4 ºC at 10 Hz (from 143.0 ºC to 137.6 ºC).

In applications of HVDC transmission systems (for ratings up to 800 kV and 8 GW) connecting large wind farms over a long distance to a utility network, the modular multilevel converter (MMC) is the best choice, because of its modularity and scalability to meet any voltage level requirements. It is imperative to regulate the MMC's submodule (SM) capacitor voltages, for the sake of proper operation of the MMC. At the same time, circulating currents have to be well controlled because of their significant influence on the ratings and power losses of the MMC. Since the SM capacitor voltages are mutually coupled with the circulating currents within the same phase leg, the control of the MMC becomes complicated. This dissertation proposes an optimized control method for the MMC based on the proposed simplified SVM scheme, which significantly improves the capacitor voltage balancing and circulating current suppression. The experimental example based on a three-phase MMC with four SMs in each arm shows that compared to the case without using the optimized control, the maximum ripple of the SM capacitor voltages is reduced by 1/6 (i.e., reduced by 16.7%) because of the optimized control method. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed method is well suited to the MMC with a large number of SMs.

7.2 Contributions

The contributions of this research are summarized as follows:

- The inherent relationship between the space vector modulation (SVM) method and the nearest-level modulation method for multilevel converters is established: the two modulation methods are functionally equivalent. An efficient and flexible modulation method for any multiphase multilevel converter is therefore proposed.
- A simplified SVM scheme for multilevel converters is proposed, which is independent of the level number of the converter and for the first time achieves the same easy implementation as phase-voltage modulation techniques. Based on two orthogonal unit-vectors that decouple the components of different phases, the proposed scheme can potentially be extended to multiphase multilevel applications.
- A modulation scheme for power loss balancing control of the three-level active neutral point clamped (ANPC) converter is developed, which significantly improves the power loss and thermal sharing among the semiconductor devices. The influence of the fundamental frequency on the thermal dynamics of the ANPC converter is also evaluated.
- An optimized control method based on the SVM scheme is proposed for the modular multilevel converter (MMC), which significantly improves the capacitor voltage balancing and circulating current suppression. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed method is well suited to the MMC with a large number of submodules.

Six journal articles, three U.S. patents, and ten conference papers have resulted from this dissertation work, as listed below:

Journal Articles:

[1] **Y. Deng**, Y. Wang, K. H. Teo, M. Saeedifard, and R. G. Harley, "Optimized control of the modular multilevel converter based on space vector modulation," *IEEE Transactions on Power Electronics*. [Under Review]

[2] **Y. Deng**, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Transactions on Power Electronics*. [Online]. Available: http://ieeexplore.ieee.org/.

[3] **Y. Deng**, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1873-1886, March 2016.

[4] **Y. Deng** and R. G. Harley, "Space-vector versus nearest-level pulse width modulation for multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2962-2974, June 2015.

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[6] L. He, J. R. Mayor, R. G. Harley, H. Liles, G. Zhang, and **Y. Deng**, "Multi-physics modeling of the dynamic response of a vacuum automatic circuit recloser system," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3697-3707, Nov./Dec. 2014.

Patents:

[1] K. H. Teo and **Y. Deng**, "Maximum power point tracking for photovoltaic power generation system," U.S. Patent. [Allowed on March 14, 2016; Application Serial No. 14/020,940]

[2] K. H. Teo and **Y. Deng**, "DC-link voltage balancing control for multilevel inverters," U.S. Patent #2014/0050000 A1, published Feb 20, 2014.

[3] K. H. Teo and **Y. Deng**, "Space vector modulation for multilevel inverters," U.S. Patent #2014/0016382 A1, published Jan 16, 2014.

Conference Papers:

[1] J. Dai, G. K. Venayagamoorthy, R. G. Harley, **Y. Deng**, and S. M. Potter, "Adaptive-critic-based control of a synchronous generator in a power system using biologically inspired artificial neural networks," in *Proc. International Joint Conference on Neural Networks (IJCNN)*, Killarney, Ireland, July 2015, pp. 1-8.

[2] **Y. Deng**, M. Saeedifard, and R. G. Harley, "An optimized control strategy for the modular multilevel converter based on space vector modulation," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, March 2015, pp. 1564-1569.

[3] **Y. Deng**, M. Saeedifard, and R. G. Harley, "An improved nearest-level modulation method for the modular multilevel converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, March 2015, pp. 1595-1600.

[4] **Y. Deng**, G. K. Venayagamoorthy, and R. G. Harley, "Optimal allocation of power routers in a STATCOM-installed electric grid with high penetration of wind energy," in *Proc. Clemson University Power Systems Conference (PSC)*, Clemson, SC, March 2015, pp. 1-6.

[5] **Y. Deng**, Y. Wang, K. H. Teo, and R. G. Harley, "Space vector modulation method for modular multilevel converters," in *Proc. Annual Conference of IEEE Industrial Electronics Society (IECON)*, Dallas, TX, Oct./Nov. 2014, pp. 4715-4721.

[6] **Y. Deng**, G. K. Venayagamoorthy, and R. G. Harley, "Optimal utilization of STATCOM devices in a power system with high penetration of wind generation," in *Proc. Clemson University Power Systems Conference (PSC)*, Clemson, SC, March 2014, pp. 1-6.

[7] **Y. Deng**, K. H. Teo, and R. G. Harley, "A fast and generalized space vector PWM scheme and its application in optimal performance investigation for multilevel inverters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Denver, CO, Sept. 2013, pp. 3977-3983.

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[10] **Y. Deng**, K. H. Teo, and R. G. Harley, "Generalized DC-link voltage balancing control method for multilevel inverters," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, March 2013, pp. 1219-1225.

7.3 Recommendations for Future Work

7.3.1 Development of SVM Schemes for Multiphase Multilevel Converters

Chapter 4 has introduced a general approach to construct the orthogonal unit-vectors for any multiphase systems, but due to the research objectives of this dissertation only the simplified SVM for three-phase multilevel converters has been developed. It would be very useful to develop a simplified SVM scheme for multiphase multilevel converters, since existing multiphase multilevel SVM schemes are difficult to implement [62] [63]. The orthogonal unit-vectors introduced in Chapter 4 have provided a good start. The final objective is to implement the multiphase multilevel SVM in the same way as for the phase-voltage modulation techniques while maintaining significant flexibility, as demonstrated in Chapter 4 for the three-phase converters.

7.3.2 Control of Back-to-Back ANPC Converters for DFIG Wind Turbine Generators under Fault or Islanding Conditions

The power loss balancing method for the three-level ANPC converter has been proposed in Chapter 5. It would be interesting to apply the proposed ADF-PWM (adaptive doubled frequency PWM) to control back-to-back ANPC converters for DFIG wind turbine generators, especially under short-circuit faults or islanding conditions. In those conditions, the converters (especially the rotor side converter) experience significantly larger currents than in normal operating conditions [100] [101]. It would be of great value to investigate how much improvement the proposed ADF-PWM could create for the safe operating areas (SOAs) and thermal limits of the converters.

7.3.3 Power Loss Balancing Control for the MMC

Though most research for the MMC at this time is focused on the capacitor voltage balancing and circulating current suppression, the MMC also suffers from unequal power loss distribution among its submodules or semiconductor devices, similar to the ANPC converter. An idea, inspired by the power loss balancing control for the ANPC converter, is to adaptively select the ON- and OFF-state submodules of the MMC according to the submodules' thermal performance. Note that since the power loss balancing control may conflict with the capacitor voltage (or circulating current) control, it would be a key point to appropriately coordinate the two control objectives.

7.3.4 Wide-Area Coordinated Control for a Power System with ANPC-based DFIG Wind Turbine Generators and MMC-based HVDC Systems and FACTS Devices

This dissertation has proposed control methods for the ANPC converter (for controlling a single wind turbine generator) and the MMC (for energy transmission of large wind farms). The next step is to analyze a power system with ANPC-based DFIG

wind turbine generators and MMC-based high voltage direct current (HVDC) transmission systems and flexible AC transmission systems (FACTS) devices, such as static synchronous compensators (STATCOMs) [102] [103]. In order to optimally utilize the power electronic converters, a wide-area coordinated control similar to [51] could be developed.

APPENDIX A ADDITIONAL INFORMATION FOR THE PROPOSED SVM SCHEME IN CHAPTER 4

A.1 An Alternative Way to Detect the Nearest Three Vectors

Similar to (4.10), the candidate switching states for the other two nearest vectors can also be directly obtained as follows

$$\begin{bmatrix} S_{a2} \\ S_{b2} \\ S_{c2} \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \text{mid}(x, y, -y) \\ y - \text{mid}(x, y, -y) \\ -y - \text{mid}(x, y, -y) \end{bmatrix} \right) \tag{A.1a}$$

$$\begin{bmatrix} S_{a3} \\ S_{b3} \\ S_{c3} \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \max(x, y, -y) \\ y - \max(x, y, -y) \\ -y - \max(x, y, -y) \end{bmatrix} \right) \tag{A.1b}$$

where mid(x, y, -y) and max(x, y, -y) respectively mean the middle and maximum values among x, y, and -y; int(γ) rounds the elements of γ to the nearest integers towards minus infinity. The explanation of (A.1) is similar to the demonstration in (4.11) and Figures 4.6 and 4.7. Correspondingly, (A.1b) detects the vertex of the modulation triangle that is farthest from the origin of the space vector diagram.

For any candidate switching state $S_aS_bS_c$ given by (A.1), all the available switching states of the detected nearest vector can be generated [44] as

$$[N + S_a, N + S_b, N + S_c]^T, \text{ where the integer } N \in [-\min(S_a, S_b, S_c),\ n - 1 - \max(S_a, S_b, S_c)] \tag{A.2}$$

A.2 An Alternative Way to Calculate *reg*

The region number, *reg*, of the remainder vector $\boldsymbol{V}_{\text{ref}}$' in (4.18) can also be calculated as follows

$$reg = \begin{cases} 1, \ \textbf{if } (0 \le V_{ry} < \sqrt{3}V_{rx}); \\ 2, \ \textbf{else if } (V_{ry} \ge \sqrt{3}V_{rx} \textbf{ and } V_{ry} > -\sqrt{3}V_{rx}); \\ 3, \ \textbf{else if } (0 < V_{ry} \le -\sqrt{3}V_{rx}); \\ 4, \ \textbf{else if } (\sqrt{3}V_{rx} < V_{ry} \le 0); \\ 5, \ \textbf{else if } (V_{ry} \le \sqrt{3}V_{rx} \textbf{ and } V_{ry} < -\sqrt{3}V_{rx}); \\ 6, \ \textbf{else}. \end{cases} \tag{A.3}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{ref}$'/V_{dc}, respectively.

A.3 Comparison with Earlier Methods

The flowchart of the SVM method in [39] is illustrated in Figure A.1, which is obtained with reference to Figure 4.7 and (4.10). The required equations are

$$g = \frac{V_{ref(x)} - V_{ref(y)}/\sqrt{3}}{V_{dc}}, \quad h = \frac{2V_{ref(y)}}{\sqrt{3}V_{dc}} \tag{A.4}$$

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} g - \min(g, 0, -h) \\ 0 - \min(g, 0, -h) \\ -h - \min(g, 0, -h) \end{bmatrix} \right) \tag{A.5}$$

$$sgn = g + h - \text{ceil}(g) - \text{floor}(h) \tag{A.6}$$

$$s = \begin{cases} 1, \ \textbf{if } (h > 0 \textbf{ and } h \ge -g); \\ 2, \ \textbf{else if } (h \le 0 \textbf{ and } g > 0); \\ 3, \ \textbf{else}. \end{cases} \tag{A.7}$$

where g and h are the coordinates of $\boldsymbol{V}_{ref}$ in the 60º coordinate system; (A.5) is a representation of (4.10) in the 60º coordinate system; ceil(g) rounds g to the nearest integer towards infinity; floor(h) rounds h to the nearest integer towards minus infinity; s indicates the three different locations of the reference vector according to Figure 4.7. The duty cycles d_{ll}, d_{ul}, d_{lu}, and d_{uu} are defined in [39]. Note that the operation encircled by the dashed rectangle R_2 in the flowchart is easily achieved by (4.16), (4.18), and (4.19) in the proposed new scheme in Chapter 4, as highlighted by the dashed rectangle R_1 in Figure 4.10.

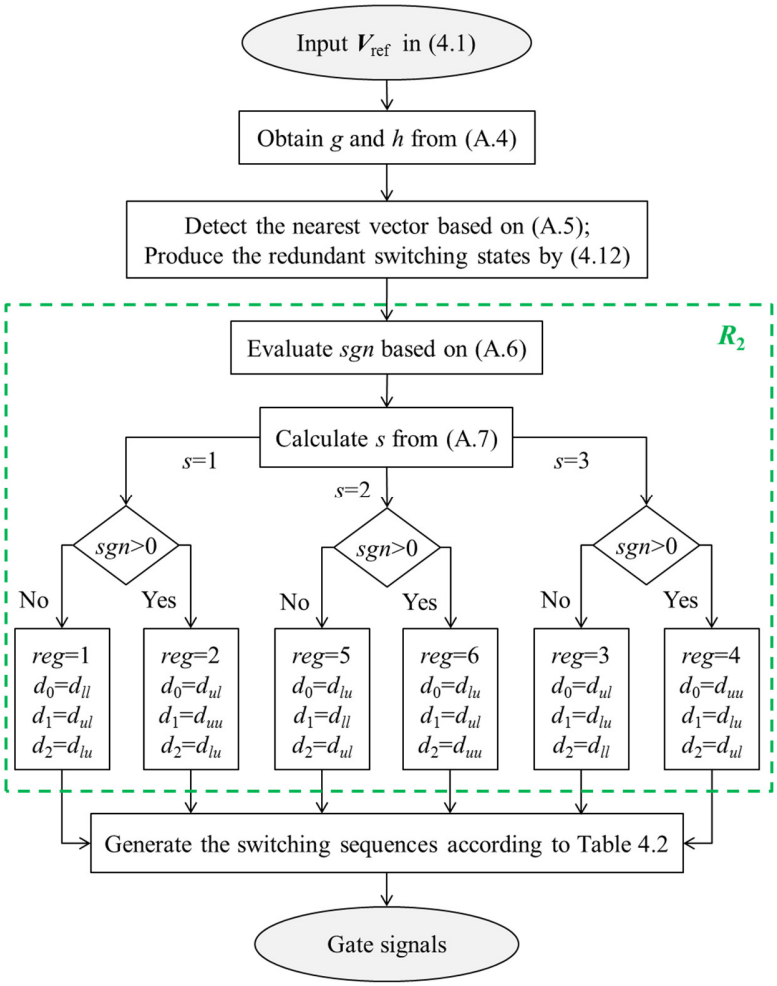


Figure A.1 Flowchart for the SVM scheme in [39].

Figure A.2 shows the detection of the nearest vector for the SVM method in [44], which requires the following steps:

1) Determines the initial virtual level number n_0, or the hexagon (H_0) that encloses the original reference vector;
2) Detects the n_0-1 level hexagon (H_1) that contains the reference vector, and updates n_0 to n_0-1;
3) Shifts the origin (O) of the reference vector to the center vertex (O_1) of the detected hexagon, which yields a new reference vector;

4) Calculates the switching state for the center vertex (O_1) of the detected hexagon, based on the shifting ($\boldsymbol{OO}_1$) of the reference vector;

5) Repeats the steps 2) - 4) for the new reference vector, until a two-level hexagon (H_3) that encircles the vertex of the original reference vector is found.

This procedure depends on the level number of the converter and the location of the reference vector, and requires iterative calculations. These iterative calculations lead to extra computational effort, but are simply replaced by (4.10) in the proposed new scheme. Therefore, the proposed new scheme is faster than the method in [44] in most cases, i.e., when the reference vector is located outside the innermost two-level hexagon (the hexagon H_S shown in Figure A.2). The computational burdens of the method in [44] and the proposed new scheme are equivalent only when the reference vector is enclosed by the innermost two-level hexagon H_S.

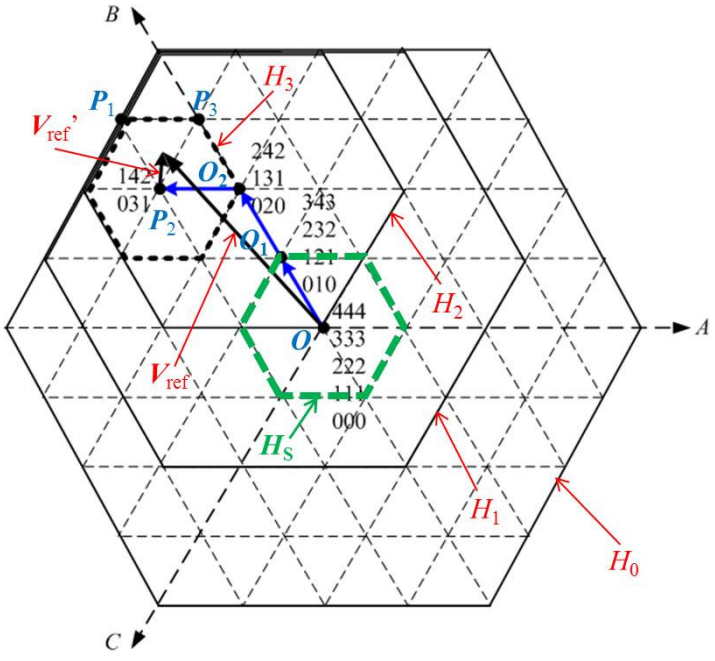


Figure A.2 Nearest vector detection of the SVM scheme in [44].

APPENDIX B ADDITIONAL INFORMATION FOR THE POWER LOSS AND THERMAL ANALYSIS IN CHAPTER 5

The parameters of the FF225R17ME4 IGBT/Diode are presented in Table B.1. The average, peak, and ripple of the junction temperatures in Figures 5.12 and 5.13 are summarized in Tables B.2 and B.3, respectively.

Table B.1 Parameters of the FF225R17ME4 IGBT/Diode

Parameter (IGBT)	Value (IGBT)	Parameter (Diode)	Value (Diode)
E_{on}	72 mJ (I_{s0}=225 A, V_{s0}=900 V)	E_{rec}	69 mJ (I_{d0}=225 A, V_{d0}=900 V)
E_{off}	83.5 mJ (I_{s0}=225 A, V_{s0}=900 V)	V_{fd0}	0.942 V
V_{fs0}	1.04 V	R_d	0.0045 Ω
R_s	0.0063 Ω	R_{th1}	0.01008 K/W
R_{th1}	0.0033 K/W	R_{th2}	0.03808 K/W
R_{th2}	0.015217 K/W	R_{th3}	0.10064 K/W
R_{th3}	0.070217 K/W	R_{th4}	0.0112 K/W
R_{th4}	0.01045 K/W	τ_1	0.0008 s
τ_1	0.0008 s	τ_2	0.013 s
τ_2	0.013 s	τ_3	0.05 s
τ_3	0.05 s	τ_4	0.6 s
τ_4	0.6 s		

Table B.2 Details of the Junction Temperatures of S_{x2} in Figure 5.12

	Average (ºC)	Peak (ºC)	Ripple (ºC)
NPC (50 Hz)	127.0	132.3	9.9
ANPC, DF-PWM (50 Hz)	125.1	130.9	10.2
ANPC, ADF-PWM (50 Hz)	123.0	127.9	8.9
NPC (10 Hz)	126.8	145.5	32.8
ANPC, DF-PWM (10 Hz)	124.3	143.0	31.8
ANPC, ADF-PWM (10 Hz)	122.1	137.6	27.3

Table B.3 Details of the Junction Temperature of S_{x2} in Figure 5.13 When the Optimal V_{com} is Applied

	Average (ºC)	Peak (ºC)	Ripple (ºC)
ANPC, DF-PWM, optimal V_{com}	123.9	129.1	9.3
ANPC, ADF-PWM, optimal V_{com}	121.9	126.0	8.2

APPENDIX C ADDITIONAL INFORMATION FOR THE PROPOSED CONTROL METHOD OF THE MMC IN CHAPTER 6

C.1 Derivation of (6.5) and (6.6)

When the buffer inductors are coupled as in Figure 6.3, (6.1a) and (6.1b) respectively become

$$v_a = V_{dc} - u_{ap} - L_0 \cdot di_{ap}/dt - R_0 \cdot i_{ap} - M \cdot di_{an}/dt \quad \text{(C.1a)}$$

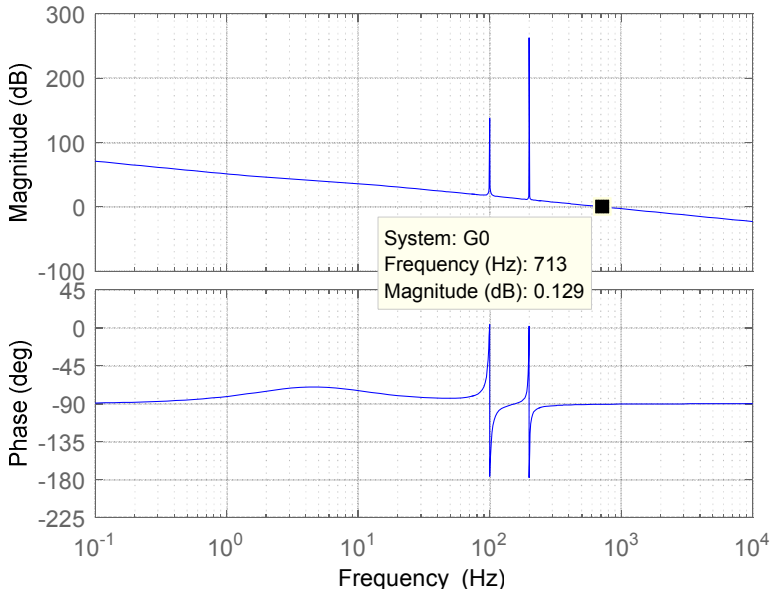
$$v_a = u_{an} + L_0 \cdot di_{an}/dt + R_0 \cdot i_{an} + M \cdot di_{ap}/dt \quad \text{(C.1b)}$$

Summation of (C.1a) and (C.1b) yields (6.5), while subtracting (C.1b) from (C.1a) leads to (6.6).

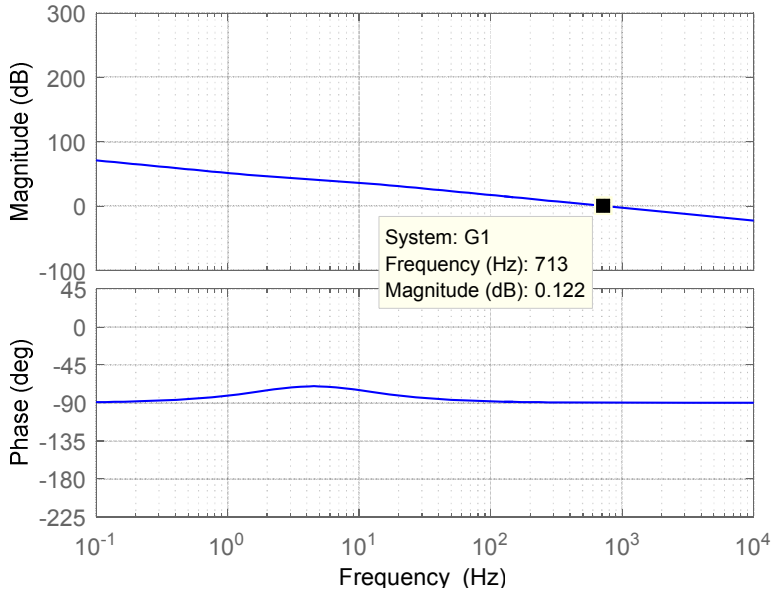
C.2 Analysis of the Circulating Current Controller

Based on the parameters of the MMC in Table 6.1 and the control parameters in Table 6.2, the Bode diagram of the open-loop transfer function in (6.13) is shown in Figure C.1(a). The bandwidth of the controller is about 700 Hz, and the phase margin is around 90º.

Figure C.1(b) shows the Bode diagram of the circulating current controller when the resonant controllers are unused, i.e., only applying the proportional-integral (PI) controller. It is observed that the resonant controllers have very narrow bandwidths. They only affect the harmonics around the resonant frequencies, as the two spikes shown in Figure C.1(a). Therefore, a general way to design the circulating current controller is selecting the PI control parameters first and then adding the resonant controllers.



(a)



(b)

Figure C.1 Bode diagram of the circulating current controller: (a) with the resonant controllers; (b) without the resonant controllers.

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